Foundation Fieldbus 总线协议执行器

解决方案

V1.0

沈阳中科博微自动化技术有限公司

2014-06-23

目录

解决方案简介

企业决定是否开发基于 Foundation Fieldbus（一下简称 FF）总线协议的执行器产品？涉及到企业产品和技术发展战略、企业现有核心技术及技术发展战略。

影响企业决策者的因素有如下几点：

- 市场的需求，无奈的现状，国外品牌的天下
- FF 总线协议的执行器开发涉及企业技术战略，影响企业现有产品技术基础与发展
- FF 总线协议的执行器产品的批量成本及利润空间
- FF 总线协议的执行器解决方案的选择，一次性投入？风险？

1. 市场：需求？现状？

(1) 市场需求：需求主要来自：

- ▼ 在一些行业项目中（电力、石油化工、水泥、制药……）， FF 技术占有一定优势，用户要求系统、设备采用 FF 技术。
- ▼ 支持 FF 技术的控制系统（等采用现场总线技术（EMERSON、ABB…… PLC、DCS ）的普遍应用。
- ▼ 企业产品、系统技术提升需求（总线仪表替代模拟仪表）

现场总线技术的应用发展，对国产现有现场设备及仪表提出新的要求。

由于现场总线技术的开放性，为国产现场设备及仪表提供新的市场机会。

(2) 目前国内 FF 总线协议的执行器市场状况

国内开发 FF 总线协议的执行器主要集中在以下几种应用行业：

- ▼ 主要应用行业：电力、钢铁、水泥、石油化工
- ▼ 目前主要使用的通信网络：MODBUS、FF

(3) 用户选用国产 FF 产品的动机

用户是否会选用国产 FF 产品？动机是什么？

- ▼ 价格因素
- ▼ 产品品牌、良好的应用业绩和信誉

▼ 特殊技术指标需求及技术服务

▼ OEM 定制产品：高性能价格比

⑷ 促使企业开发 FF 产品的动力

动力之一：市场对产品的需求

系统现场总线选用 FF，由于：

A、价格因素

B、产品品牌、良好的应用业绩和信誉

C、特殊技术指标需求及技术服务

D、OEM 定制产品以求得高性能价格比

市场（用户）要求提供 FF 产品是促使企业开发 FF 产品的动力之一。

动力之二：企业产品技术升级，提高竞争力的动力

比较：MODBUS、CAN、FF、Ethernet

对国内企业来说，选择 FF 技术作为企业产品网络技术升级方案是现实的明智之举。

动力之三：使企业产品能够与国际知名品牌控制系统连接，开拓市场范围。

2. FF 产品开发与企业现有产品技术基础与发展的关系

企业发展规则：总是要追求产品技术升级，以提高竞争力。

选择那种现场总线作为企业产品网络技术升级？与企业现有产品技术基础与发展有关。

比较 MODBUS、CAN、FF、Ethernet 几种可选方案

MODBUS：已广泛采用

问题：通信速率、可靠性、标准化。。。。。。

市场要求：企业产品技术升级、标准化、与大系统的连接；

可选方案：

⑴ CAN（DeviceNet、CANOpen）：

优点：成本低、容易过渡；

主要问题：CAN 在大数据量、高功能要求中的技术局限性

⑵ Ethernet（PROFINet、 Ethernet/IP、Modbus/TCP）：

优点：技术先进；

主要问题：要求很高的产品软硬件平台、产品技术升级出现断代

⑶ FF 技术指标先进、容易进入高端市场

对国内企业来说，选择 FF 技术作为企业产品网络技术升级方案是现实的明智之举。

3. 产品技术经济：产品批量成本、利润？

⑴ 单台成本核算问题：一个 FF 设备，允许增加成本?

FF 仪表售价比原售价增加多少用户（市场）能够接受， 也就是说，即使我们产品技术升级，也不指望得到附加利润情况下，由于增加现场总线而增加的成本只能占原售价的 20%～40%。否则，用户会认为增加现场总线功能成本过高，不愿意接受现场总线方案。

根据 FF 技术成本计算，一个 FF 设备增加成本: 300~500 元左右。

由下表可知，原售价 2000 元以下的设备不适合选用 FF 技术，应该选用 MODBUS、CAN 的成本较低的技术。

⑵ 系统成本核算

向用户推荐 FF 系统方案时，与传统方案、其他方案相比是否具有竞争性？

① 与 MODBUS、CAN 等系统相比

优势：技术先进、速率高、可靠性高、技术规范、与国际系统兼容；

不足：主站成本高、网络站点数受限、网络部件成本增加（电缆、接头、中继）、安装维护成本略有上升。

② 与传统方案（PLC 及 I/O 接线）相比

优势：现场总线的优势明显；

不足：成本（造价、安装、维护）不一定高？主要是用户接受新技术的能力（技术准备、技术管理。。。。

4. FF 总线协议的执行器解决方案的选择，一次性投入？风险？

⑴ 自己开发总线通信板卡？还是购买市场上成熟的总线板卡？

对于国内企业来说购买市场上成熟可靠的总线板卡是最佳首选，如有能力也可以自主研发。

(2) 自己开发 FF 通信协议栈软件？还是购买经过测试认证的商业通信协议栈软件？

FF 通信协议栈软件得技术要求较高，购买经过测试认证的商业通信协议栈软件可以很好的解决通信带来的技术问题。

(3) 自己开发功能块应用软件？还是购买经过测试认证的商业功能块应用软件？

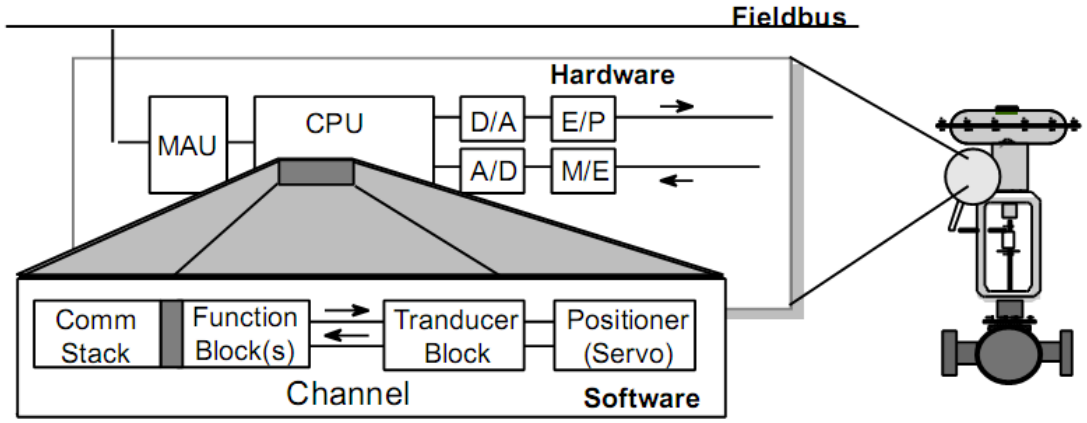
经过认证的商业功能块软件可以节省设备的研发时间，可以方便快捷的实现功能块需求。

(4) 自己编写变换块程序？还是购买服务由专业团队定制开发？

专业团队定制开发变换块程序可以加快研发的进程，可以很好的实现用户的功能设计。

用户需求描述及分析

针对不同的用户要求需要不同的解决方案相适应，首先看一看典型的 FF 执行器基本组件，如下图所示：



MAU： Medium Attachment Unit

E/P： Electric to Pneumatic Converter

M/E： Mechanical to Electric Transducer

由于各个厂商的技术能力不同，因此用户的需求也很不相同。

1. 典型的用户需求有以下几种：

▼ 用户已经具备执行器，但没有智能通信板卡，处于模拟设备阶段；

▼ 用户已经具备智能通信板卡（MODBUS、HART），但是没有 FF 总线技术；

2. 传统开发模式：

▼ 难度大、投入大、周期长、调试困难

3. 国外主流开发模式：技术集成

▼ 成熟可靠、快速响应市场、测试费用少

4. 与传统产品设计相似

▼ 针对需求设计产品的外观尺寸，所需要的部件。

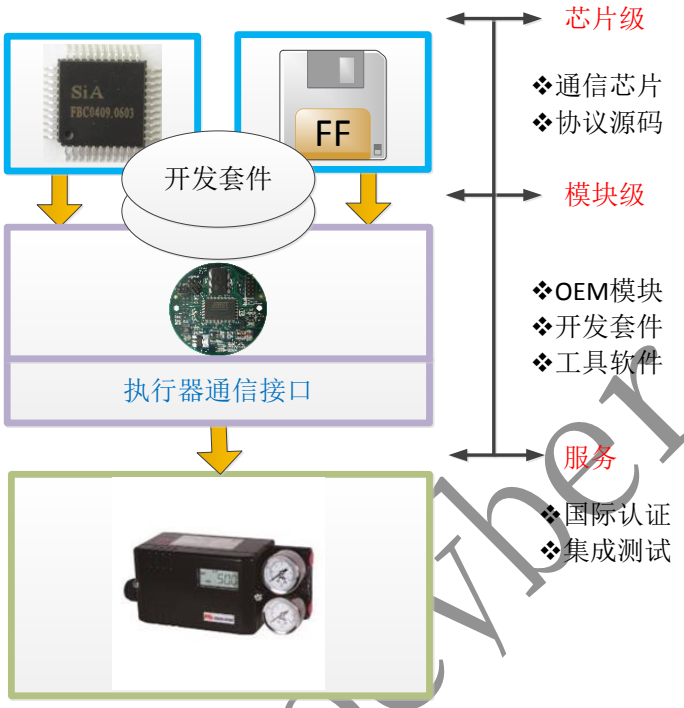
- ▼ 项目管理很重要。需要管理人具有丰富的现场总线产品开发和应用的经验，以便合理安排开发时间、开发资源和后期的测试。

5. 与传统产品设计不同

- ▼ 总线产品要远比传统产品功能复杂，要综合考虑，合理利用已有的资源和技术，不一定要一切从头做起。
- ▼ 总线产品的通信协议要求具有高度的一致性和时间确定性。因为通信网络既是控制系统，控制信号被分散到网络上的设备中。不像 DCS 和 PLC 那种集中控制设备。
- ▼ 总线产品的功能要求具有很好的可互操作性，来自不同厂商的同类设备可以实现互换而不影响应用。
- ▼ FF 基金会要求所有 FF 产品通过协议栈的一致性测试和功能块的互操作测试。
- ▼ 复杂的功能和严格的认证测试对开发总线产品提出了更高的要求。

总体设计

针对用户不同层次的需求我们可以提供不同层次的解决方案：



1. 芯片级

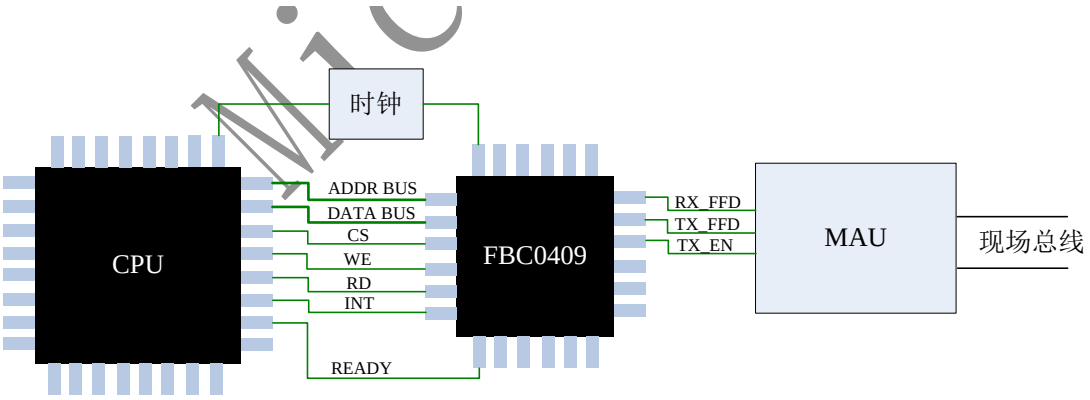
- ▼ 购买协议源码进行独立开发，用户后续只需要购买芯片及授权；
- ▼ 购买开发套件进行独立开发，用户后续只需要购买芯片及授权；
- ▼ 购买板卡授权，独立制版，用户后续只需要购买芯片及授权；
- ▼ 面向用户：
  - 具备较强开发能力
  - 以协议使用和辅助开发为目的

2. 模块级

- ▼ 标准 OEM 开发，用户后续需要购买 FF 通信板卡；
- ▼ 面向用户：
  - 具备一定开发能力
  - 能够开发或提供执行器仪表卡
  - 提供通讯或访问接口

3. FBC0409

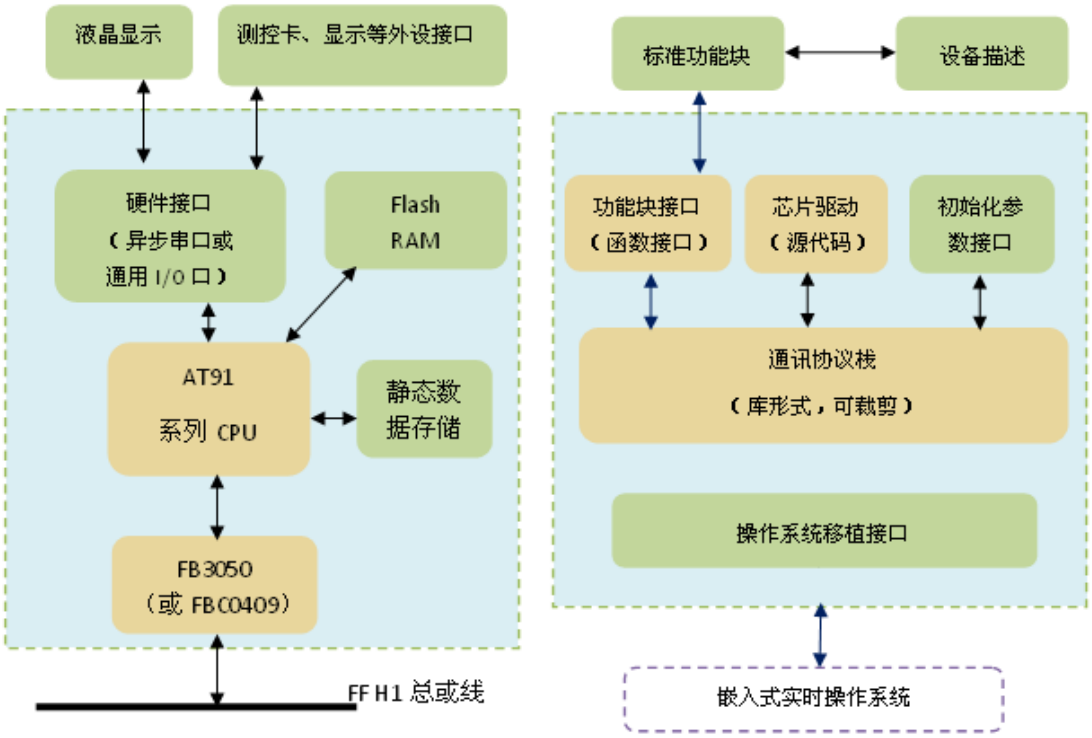
- 符合 IEC 61158-2 规范
- FF H1 总线
- 具备物理层和部分链路层功能（总线地址自动识别）
- 具有集成度高、外围电路简单，占用空间小
- 芯片管脚数量 44
- 存储器容量 4K SRAM
- 低功耗设计
- 国外同类产品：静态功耗 100uA
- FBC0409：静态功耗 60uA
- 可靠性测试
- 31.25Kbit/S 数据传输速率，曼彻斯特编码
- 禁止闲谈电路，避免接收或发送长时间占用线路
- 线路极性自动识别及校正
- 2 通道 DMA 控制器，支持发送、接收、目的地址识别
- 总线仲裁机制，确保 CPU 正确访问内部 SRAM
- 工作温度：-40~85℃



FBC0409 典型应用电路

4. FF H1 开发套件

- ▼ 硬件原理图，PCB 图
- ▼ 设备能力文件（CFF）描述模板（仅 FF H1）
- ▼ 设备描述模板源代码（DDL 语言，仅 FF H1）
- ▼ GSD/EDD 文件模板（文本文件，仅 Profibus PA）
- ▼ 功能块源代码（C 语言）
- ▼ 协议库（FF H1 或者 Profibus PA）
- ▼ 操作系统接口

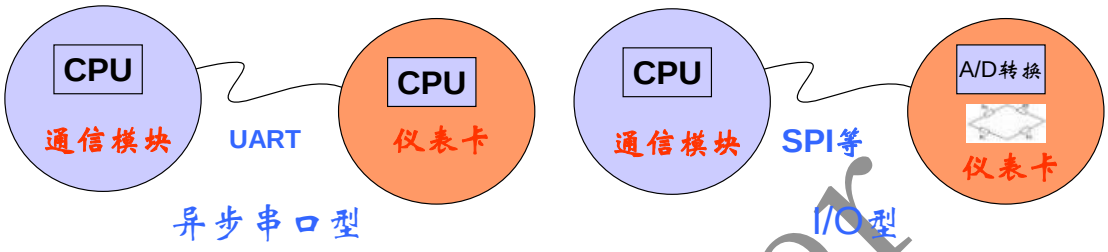


FF 开发工具硬件及软件结构

5. OEM 模块

选择现场总线通信模块进行 OEM 定制开发是快速而有效的产品开发方法之一。

- ▼ 串口方式：通过异步串口实现数据交换、自定义通信协议，采集、处理等工作主要由仪表卡上 MCU 完成
- ▼ I/O 方式：通过 I/O 接口(SPI、I2C)与 A/D、D/A 等非 MCU 类器件通信，采集、处理等工作由通信模块完成



详细设计

用户可以选择 FF 开发工具包或是标准 OEM 开发进行 FF 设备研发，简单来说标准 OEM 开发就是专业的开发团队使用 FF 开发工具针对用户需求进行的定制研发。因此 FF 开发工具包与是标准 OEM 开发有着相同的开发流程及设计结构。现在简单介绍 FF 开发工具包的设计结构。

1. FF 开发工具包提供的内容

- ▼ FF-H1 通信圆卡
- ▼ FF-H1 软件开发包
- ▼ 技术支持

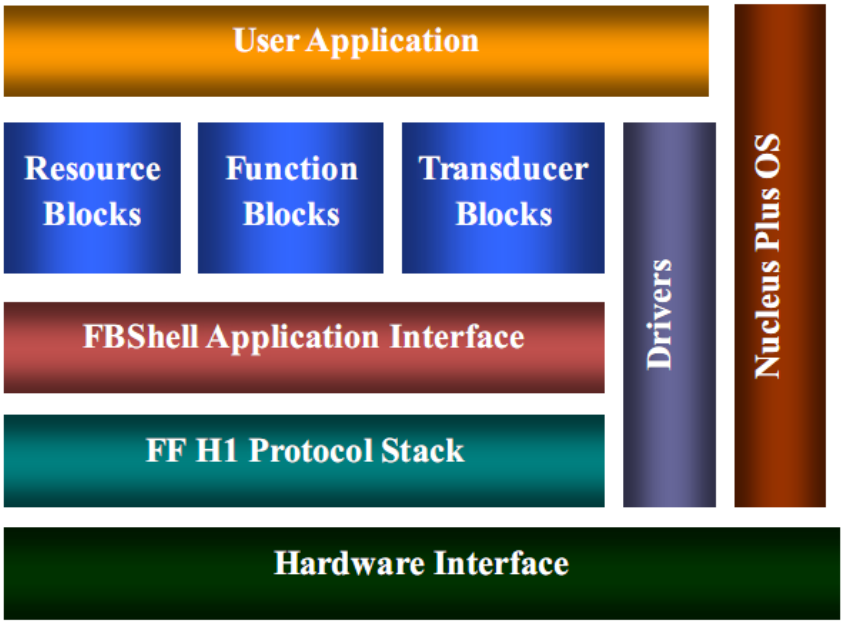
2. FF-H1 通信圆卡

- ▼ 标准 FF-H1 通信卡，提供原理图，用户可以根据具体需求进行修改。

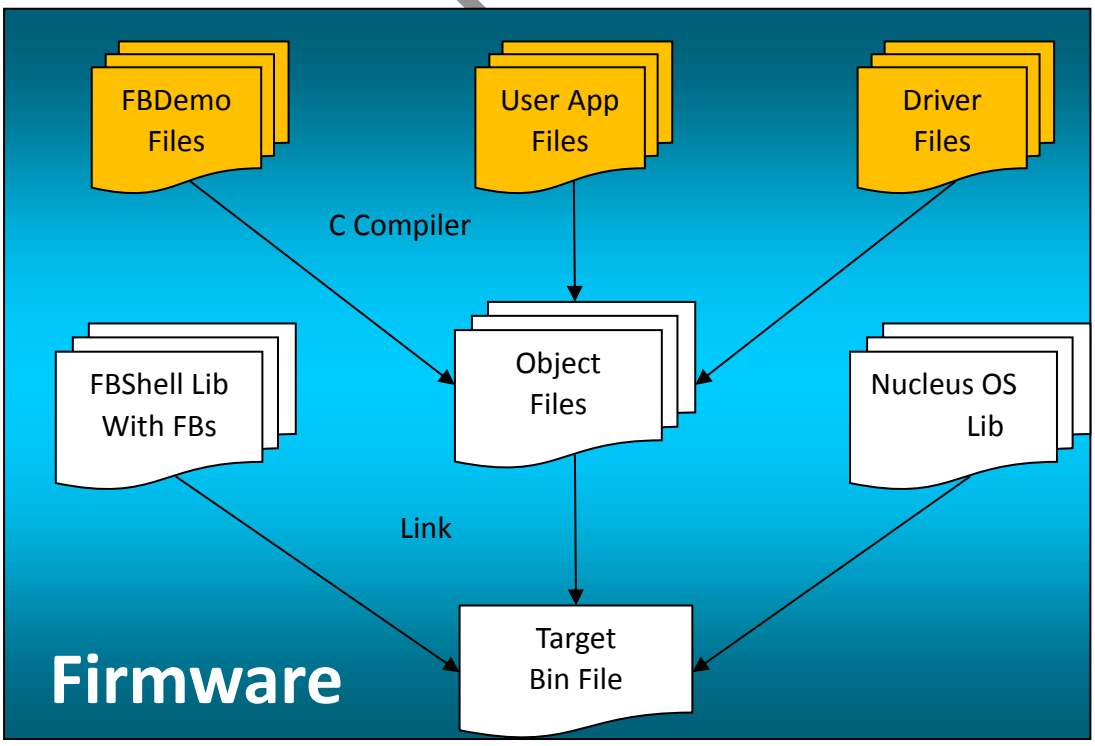
3. FF-H1 软件开发包

- ▼ 基于 FF-H1 圆卡硬件平台和 Nucleus Plus 嵌入式实时操作系统。
- ▼ 将 FF 通信协议和功能块管理封装成 FBShell 库，许多标准的功能块被包含在库中。
- ▼ 开发人员只要简单地设置一些参数即可构建一个完整的 FF H1 通信协议栈。
- ▼ 通过注册功能块类型可以在设备中实现各种功能块。
- ▼ 也可以通过 FBShell 接口开发其他的功能块。
- ▼ 提供 DD 和 CFF 文件模板。
- ▼ 提供自定义功能块开发模板。
- ▼ 提供基于 ARM 的驱动程序源码，串口通信源码等

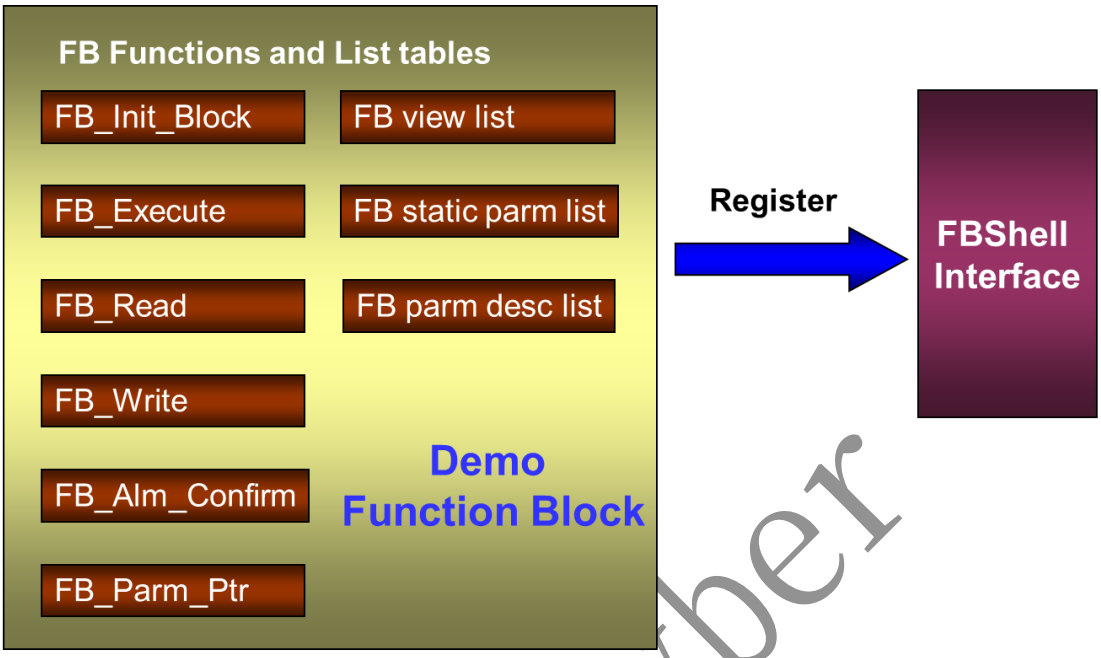
4. FF-H1 软件开发包-软件结构图



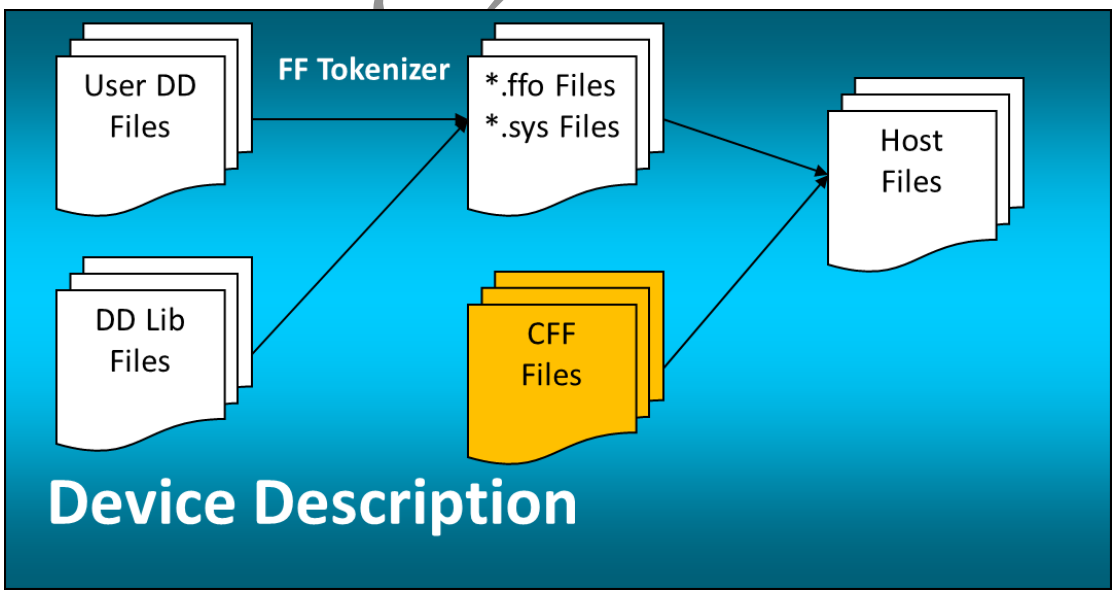
5. FF-H1 软件开发包-软件开发流程



6. FF-H1 软件开发包-功能块类型注册



7. FF-H1 软件开发包-DD&CFF 开发



8. 执行器功能块设计

执行器为执行单元，因此执行器中会支持多路的 AI、AO、DI 及 DO 功能块，而控制功能块不会太多，基本上支持 PID 功能块就做够了，具体执行器支持的 AI、AO、DI 及 DO 功能块的数量要结合实际设备确定（可参考**附录三 FF 总线功能块参数简介**进行功能块选择）。

9. 执行器变换块设计

执行器可分为模拟、离散以及模拟/离散混合三种形式，在 FF 协议规范中提供了标准定位器的变换块协议（FF-906，Positioner Transducer Block），可为用户开发 FF 执行器提供参考，由于用户的具体设备与标准参数存在差距，因此在具体开发时要进行必要的参数增减。

10.Standard Advanced Analog/Discrete Positioner Basic Device Access

Index	Parameter Mnemonic	VIEW_1	VIEW_2	VIEW_3	VIEW_4_1	VIEW_4_2	VIEW_4_3	VIEW_4_4
1	ST_REV	2	2	2	2	2	2	2
2	TAG_DESC							
3	STRATEGY				2			
4	ALERT_KEY				1			
5	MODE_BLK	4		4				
6	BLOCK_ERR	2		2				
7	UPDATE_EVT							
8	BLOCK_ALM							
9	TRANSDUCER_DIRECTORY							
10	TRANSDUCER_TYPE	2	2	2	2			
11	TRANSDUCER_TYPE_VER	2	2	2	2			
12	XD_ERROR	1		1				
13	COLLECTION_DIRECTORY							
14	FINAL_VALUE	5		5				
15	FINAL_VALUE_RANGE		11					
16	FINAL_VALUE_CUTOFF_HI				4			
17	FINAL_VALUE_CUTOFF_LO				4			
18	FINAL_POSITION_VALUE	5		5				
19	WORKING_POS	5		5				
20	WORKING_SP	5		5				
21	DEVIATION_DEADBAND				4			

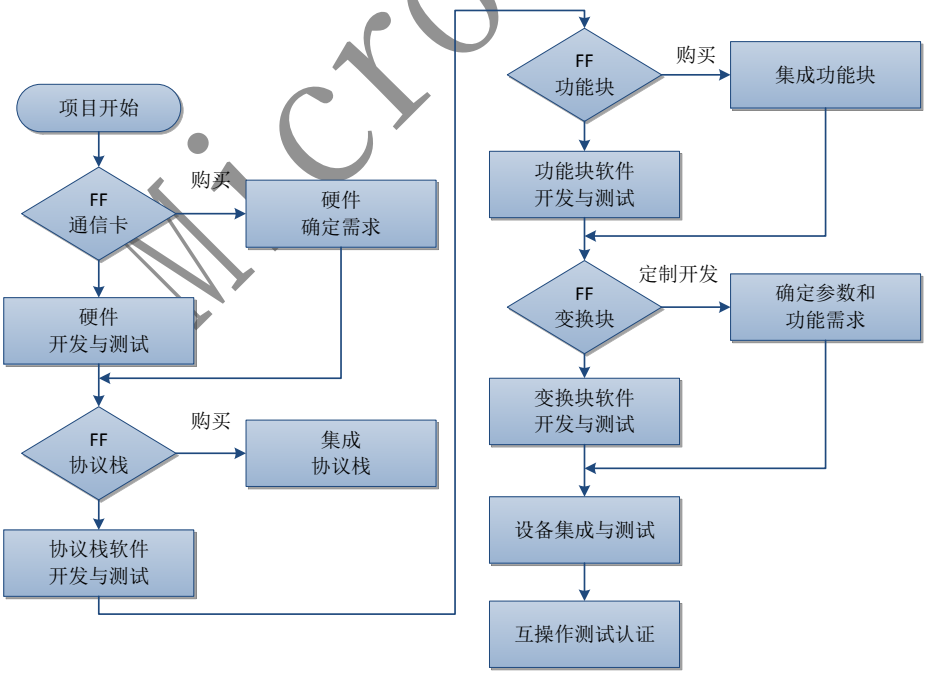
Index	Parameter Mnemonic	VIEW_ 1	VIEW_ 2	VIEW_ 3	VIEW_ 4_1	VIEW_ 4_2	VIEW_ 4_3	VIEW_ 4_4
22	DEVIATION_TIME				4			
23	DEVIATION_VALUE			4				
24	POS_ALERT_HI				4			
25	POS_ALERT_LO				4			
26	RATED_TRAVEL				4			
27	STOP_HI_POS				4			
28	STOP_LO_POS				4			
29	TRAVEL_ACCUM			4				
30	TRAVEL_UNITS				2			
31	PSNR_FSTATE_VAL		4					
32	FINAL_VALUE_D	2		2				
33	FINAL_POSITION_VALUE_D	2		2				
34	WORKING_POS_D	2		2				
35	WORKING_SP_D	2		2				
36	PSNR_FSTATE_VAL_D		2					
37	DISCRETE_STATE		2					
38	PSNR_FSTATE_OPT		1					
39	CYCLE_CNTR			4	1			
40	SIGNAL_ACTION		1					
41	READBACK_SELECT							
42	PSNR_COMMAND			2				
43	PSNR_COMMAND_STATE			2				
44	PSNR_OOS_OPT		1					
45	POS_FEATURES		2					
46	ACT_FAIL_ACTION					1		
47	ACT_MAN_ID					32		
48	ACT_MODEL_NUM					32		
49	ACT_SN					32		
50	ACT_TYPE					1		
51	VALVE_MAN_ID						32	
52	VALVE_MODEL_NUM						32	
53	VALVE_SN						32	
54	VALVE_TYPE						1	
55	XD_CAL_LOC							32
56	XD_CAL_DATE							7
57	XD_CAL_WHO							32
	Totals	41	30	57	48	100	99	73

项目实施方案

项目研发时间一般为 3 个月，在用户对功能进行检查并确认后，进行 FF 物理层测试及 ITK 预测试，完成后可进行认证申请，认证时间视用户及 FF 基金会具体时间安排为准。

计划时间（周）	阶段目标	人员 硬件/软件	备注
2	项目前期沟通，确定软硬件方案	1/1	用户需求确认
1	FF 技术培训	1/1	用户培训计划（针对 FF 开发工具包方案）
2	硬件原理图及 PCB，FF DD 预览	1/1	用户设计确认
4	硬件样卡调试，软件编程	1/1	项目研发过程
3	集成调试，样机调试	1/1	设备调试及用户功能确认
3	硬件物理层测试，电磁兼容测试，ITK 预测试	1/1	用户拿到样机
1	FF 认证测试及设备注册	1/1	开始时间视用户及 FF 基金会具体时间安排为准

FF 通信板卡项目的总体开发流程如下：



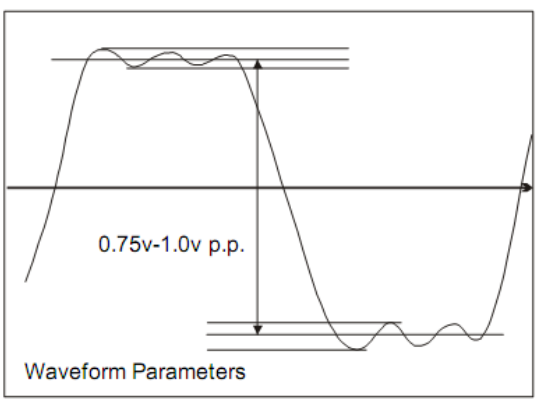
技术支持和服务

针对不同的解决方案提供的技术支持及服务不尽相同

类别	服务内容	备注
开发工具	FF 技术及开发培训为一周	
	协助用户开发一种类型的 FF 总线产品并通过认证测试	
	在维护期内用户可以免费得到开发工具包更新程序	
标准 OEM	FF 技术及开发培训为 2 天	
	维护期内可以免费得到 DD 更新	
通用服务	设备物理层测试	
	协议栈一致性测试	
	功能块互操作测试	
	FF 认证文档编写及产品认证	
	产品集成测试（支持 Emerson DeltaV 系统）	

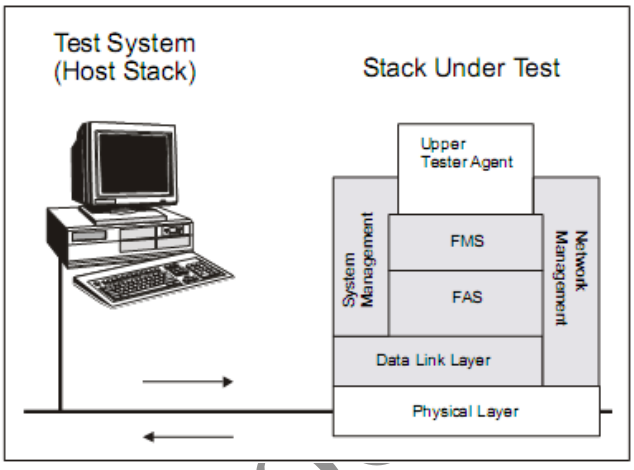
1. 物理层测试

- ▼ 物理层测试是对设备的电子特性进行测试，如供电范围，本安要求，噪声测试等等。
- ▼ FF 基金会有物理层测试的规范和测试案例。
- ▼ 可以自测也可以委托第三方测试。
- ▼ 有效的物理层测试报告是做进一步其他测试的基础，在做一致性测试和互操作测试之前都需要提交物理层测试报告。



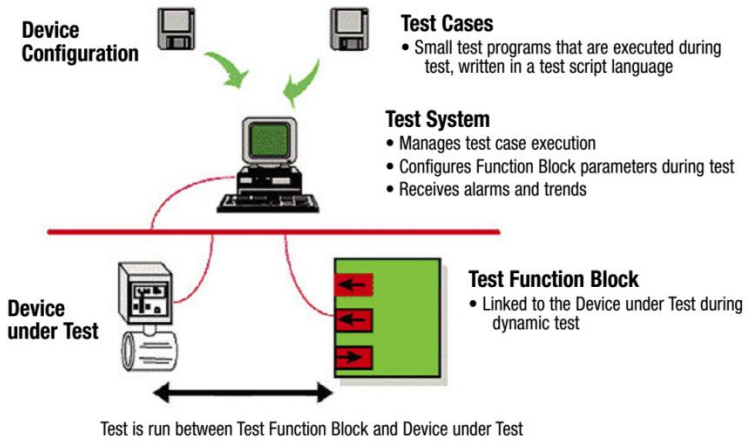
2. 一致性测试

- 一致性测试是对通信协议栈的测试，包括数据链路层测试，FAS 和 FMS 报文规范测试，系统管理和网络管理测试以及 LAS 功能测试等等。
- 通过测试的协议栈软件可以应用在其他的厂商的设备中，但要保证具有相同的硬件平台。
- FF 通信协议栈非常复杂，目前只有十几家获得认证。大部分的 FF 设备都是通过 OEM 合作的方式直接使用这些获得认证的协议栈软件。



3. 互操作测试

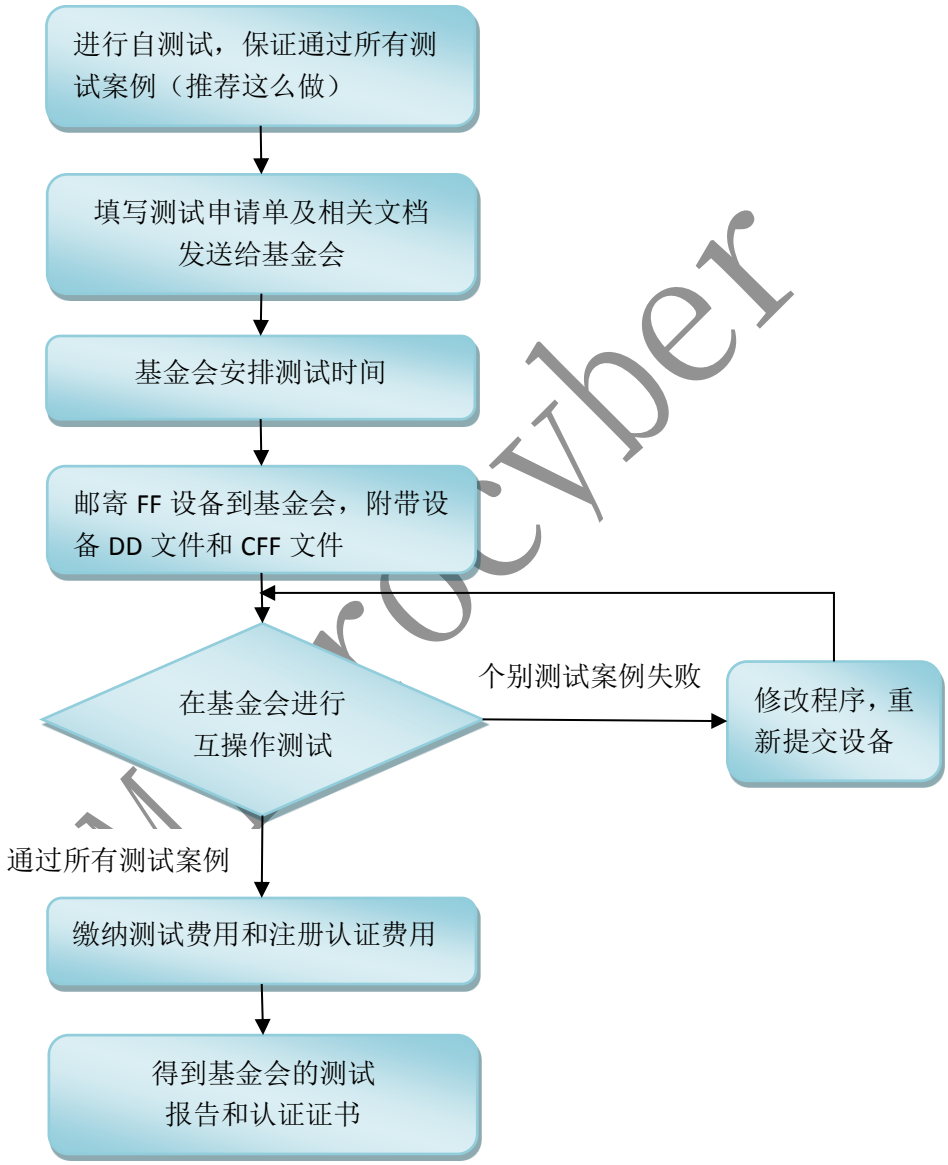
- 互操作测试主要是对 FF 设备功能块应用软件的测试。包括功能块的连接组态，模式和状态，事件和报警，趋势数据，仿真和写保护，DD 和 CFF 文件测试等等。
- FF 基金会每年都会更新功能块规范，增加一些新的功能块，相应的互操作测试规范和案例也会不断更新。



4. 产品认证

为了保证不同厂商设备的可互操作性，现场总线基金会推出了互操作测试服务。只有通过了所有的互操作测试，该设备才可以得到基金会的认证并被注册到基金会的网站上。互操作测试服务在很大程度上降低了不同厂商的设备在同一个总线系统上使用时带来的兼容性问题，因此，通过互操作测试是一个 FF 设备供应商必须要做的事情。

一个新的 FF 设备做互操作测试与认证需要按照如下流程进行。



设备通过 ITK 测试并完成设备注册后可获得设备注册证书：

FOUNDATION™
DEVICE REGISTRATION

Manufacturer:	Microcyber Inc.
Model:	NCS-IF105
Type:	4-20 mA to Fieldbus Converter
Device ITK Version:	5.0.1
Device Test Campaign:	IT056200
Test Report:	FF-527-(56200)
Stack Test Campaign:	CT0076FF
Physical Layer Test Report:	PT-279
Manufacturer ID:	0x000105
Device Type:	0x0001
Device Revision:	0x01

	Filename	CRC	ITK Version
Device Description:	0101.ffo	7CC4B577	5.0.1
	0101.sym	14321EAC	5.0.1
Capability File:	010101.cff	6F6B63DB	5.0.1

Tested Features:
Alarms and Events
Trending
Function Block Linking
Block Instantiation
Resource Block
Analog Input Function Blocks
PID Control Function Block
Input Selector Function Block
Signal Characterizer Function Block

17 September 2008
Registration Date

Richard J. Timoney
President and CEO

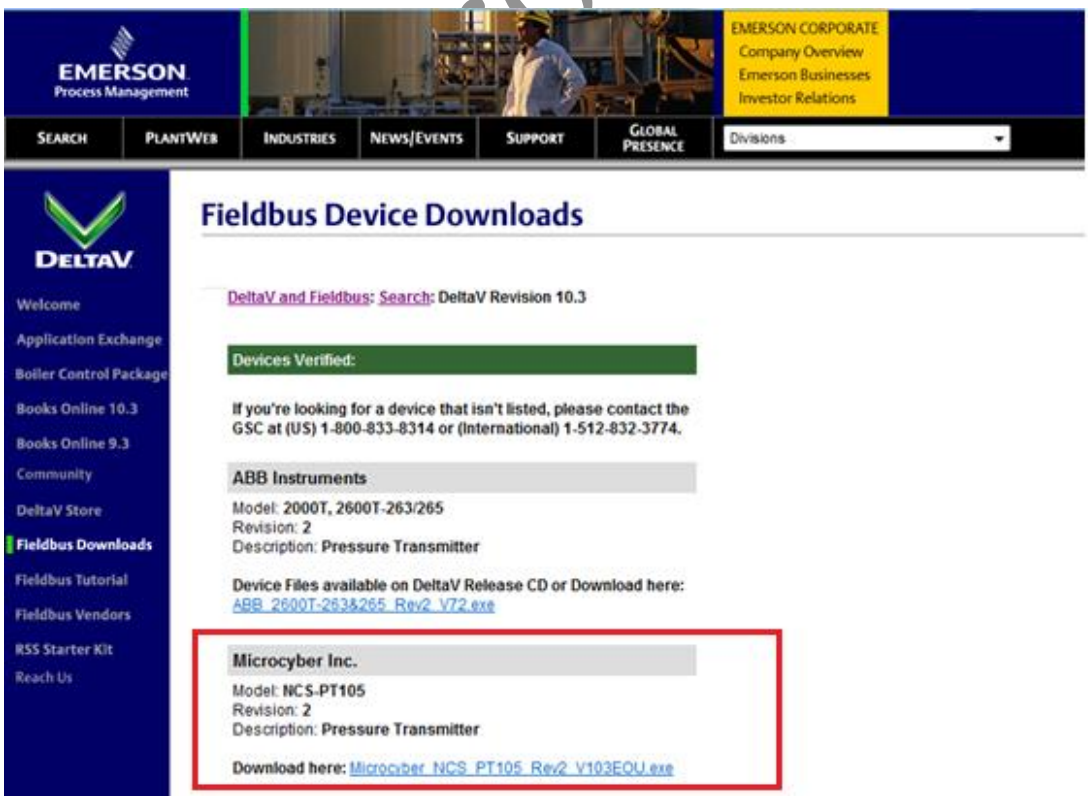
5. 产品集成测试

- 集成现场总线技术是传统 DCS 系统到新一代 DCS 系统转变的一个显著特征。
- 现场总线系统作为 DCS 系统的一个子集被集成到 DCS 控制应用中。
- 为了获得更好的设备互操作性和系统兼容性，有必要对通过认证测试的设备在专有 DCS 系统上做集成测试。
- 世界知名 DCS 厂商都免费为通过认证的 FF 设备做系统集成测试，并给出测试分析报告供设备厂商完善其设备。
- 通过集成测试的产品被认为与该 DCS 系统具有很好的兼容性，产品信息和 DD 文件会被发布到该厂商的官方网站上。

博微公司的 FF 产品通过多家 DCS 系统集成测试,通过 ABB 公司系统集成测试

Category	Vendor	Device Type	Application	Device Library [1]	Device Description (Device Type / Device Revision, DD Revision)
Pressure	ABB	2010TA, 2010TD, 2020TA,	Pressure and Level	ABB 2000T V1.0-FF	0x0089 /01,01
		2600T HI	Pressure and Level	ABB 2600T HI V1.1-FF	0x004 / 01,01
		2600T - 264	Pressure and Level	ABB 2600T-264 V2.2-FF	0x004 / 02,01
		2600T Series 26TXX, 269XX		ABB 267_269 V1.2-FF	0x008A / 02,01
		2600T - 265		ABB 2600T-265 V1.1-FF	0x0089 /02,01
	Anderson Instru-ments	FPP		Anderson Instruments FPP V1.0-FF	0x1000 / 01,01
	Dynisco	SPX series		Dynisco SPX Series V1.0-FF	0x3031 / 01,01
	Endress+Hauser	Cerabar S (PMC 631, 731; PMP 635, 731)		Endress + Hauser Cerabar S V1.0-FF	0x1007 / 05,01
		DELTABAR-S PMD230, FMD230, PMD235, FMD630, FMD633		Endress + Hauser DELTAB-S V1.1-FF	0x1009 / 02,01
		Deltapilot S		Endress + Hauser Deltapilot S V1.0-FF	0x100B / 01,02
	Foxboro	I/A series		Foxboro I/A V1.0-FF	0xBA30 / 20,01
		FCX-AX2		Fuji Electronic FCX-AX2 V1.0-FF	0x0032 / 01,01
	Honeywell	ST3000		Honeywell ST3000 V1.1-FF	0x0002 / 08,01
	Microcyber Inc.	NCS-PT105		Microcyber Inc. NCS-PT105 V1.0-FF	0x03 / 02,03
	Rosemount	3051		Rosemount 3051 V1.1-FF	0x3051 / 07,02
		3051S		Rosemount 3051S V1.1-FF	0x3051 / 14,02
		3095MV		Rosemount 3095MV V1.0-FF	0x3095 / 01,01
	Siemens	SITRANS P DSIII		Siemens SITRANS P DS V1.0-FF	0x000B / 01,01
	Smar	LD302		Smar LD302 V1.0-FF	0x0001 / 04,02

博微公司的 NCS-PT105 产品通过 EMERSON 公司 DELTAV 系统集成测试



项目预算

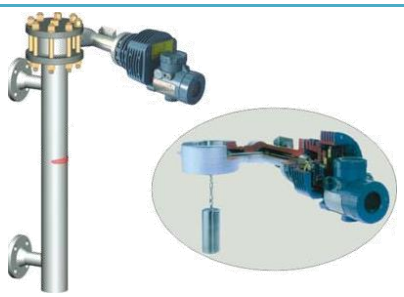
项目预算表

预算科目名称		说明	预算
FF 测试系统	NI USB-8486	FF 总线接口卡，USB 接口	30,000￥
	NI-FBUS Configurator	FF 组态软件	30,000￥
	NCS-BP105	FF 总线电源	3,000￥
	NCS-BT105	FF 终端匹配器	1,500￥
FF 认证测试	FF 会员费用	企业成为 FF 基金会会员年费	1,500$
	FF 测试费用	测试一种设备类型的费用	4,500$
	FF 设备注册费	注册一种设备类型的费用	2,500$
	设备邮寄费用	设备邮寄到 FF 基金会的费用	1,000￥

公司业绩简介

名称	类型	公司	设备图片
EIM DCM Fieldbus Actuator	Electric Actuator	Emerson Process Management	
A2-ACM-H1	Electronic Actuator - Valve Positioner	AMFLOW	
EX210-FF	Valve Actuator Positioner	Orange Instruments Limited	
SS	Smart Valve Positioner	Power-Genex Ltd.	

名称	类型	公司	设备图片
FlowMaster EM Flow Meter	Flow	ChongQing ChuanYi Automation Co., Ltd.	
M8000 Actuator	Electric Actuator	ChongQing ChuanYi Automation Co., Ltd.	
PDS	Pressure Transmitter	ChongQing ChuanYi Automation Co., Ltd.	
DDTOP-F	Fieldbus Flow Transmitter	Dandong Top Electronic Instrument Co., Ltd.	

名称	类型	公司	设备图片
DDTOP-L	Fieldbus Liquid Level Transmitter	Dandong Top Electronic Instrument Co., Ltd.	
Autrol APT3500	Pressure Transmitter	Duon System Co., Ltd.	
NCS-TT108	Temperature Transmitter	Microcyber Corporation	
NCS-IF105	4-20 mA to Fieldbus Converter	Microcyber Corporation	

名称	类型	公司	设备图片
NCS-FI105	FI Converter	Microcyber Corporation	
NCS-PT105	Pressure Transmitter	Microcyber Corporation	
NCS-LD105	H1/HSE Linking Device	Microcyber Corporation	

附录一 FBC0409 芯片数据手册

1. General description

FBC0409 ff-bus controller conforms to IEC 61158 Fieldbus physical layer definition, supports typical embedded CPU and MCU, and satisfies the demands of high performance FF-Bus masters or slavers.

FBC0409 contains Manchester data encoder and decoder on chip. It requires only a medium interface and external filter for connection to a Foundation Fieldbus system, and automatically correct line polarity. FBC0409 also contains 4k bytes build-in data RAM, applying DMA controller. Receiving and transmitting of FF-Bus data and looking up of received address are done without CPU intervening. Enough Rx and Tx data status is available in status registers of FBC0409, such as status of line operation, code error, frame loss, frame collision.

FBC0409 ff-bus controller realized a portion of data-link layer function.：Tx/Rx frame check sequence (FCS), 16 bits 1MS timer, 16 bits 1/32MS timer, 16 bits octet timer, frame code decoding and address recognizing.

2. Features

FBC0409 is designed for FF-Bus physical and part data link communication functions, details list below:

- Supports line data rate 31.25K BIT/S；
- Build-in Manchester Encoder/Decoder；
- Transmitter Jibber inhibit, receiver super long frame inhibit;
- Automatic parity recognize and correct;
- Message type and destination address detection automatically;
- Automatic transmitter and receiver frame check;
- Build-in three channels DMA controller，used to control data transmitting, receiving and address recognization looking up table memory management;
- 4k bytes asynchronous SRAM internal as communication buffer for transmitting, receiving and address lookup table memory;
- Build-in bus arbiter, CPU accessing internal SRAM correctly;
- Data link layer timer (1ms、1/32 ms、octet time timer);
- Designed lots of useful interrupt and status Registers;
- Compatibility with INTEL、ARM serials CPU；
- Internal loop back for test;
- STAND BY feature;
- Operating temperature range：-40℃～85℃
- Power consumption：<600UA;

- Available in 44-pins TQFP package;
- Length of Preamble, Start and Stop delimiter under software controlled

3. Definition

Term	Definition
FB	FOUNDATION FIELD BUS
FBC	FOUNDATION FIELD BUS CONTROLLER
IEC	INTERNATIONAL ELECTRONIC COMMITTEE
MAU	MEDIUM ATTACH UNIT
DMA	DIRECT MEMORY ACCESS
FCS	FRAME CHECK SEQUENCE

Table 1 definition

4. Typical Application

Chip FBC0409 was designed as FF-Bus communication controller, following is its typical application.

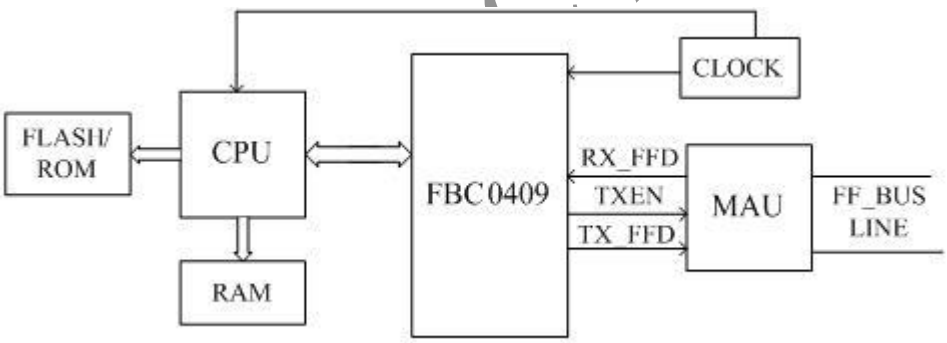


Figure 1 FBC0409 controller typical application

5. PIN description

FBC0409 is packaged in a 44-pins TQFP package and body size is 10MM X 10MM， pins pitch of 1.8MM.

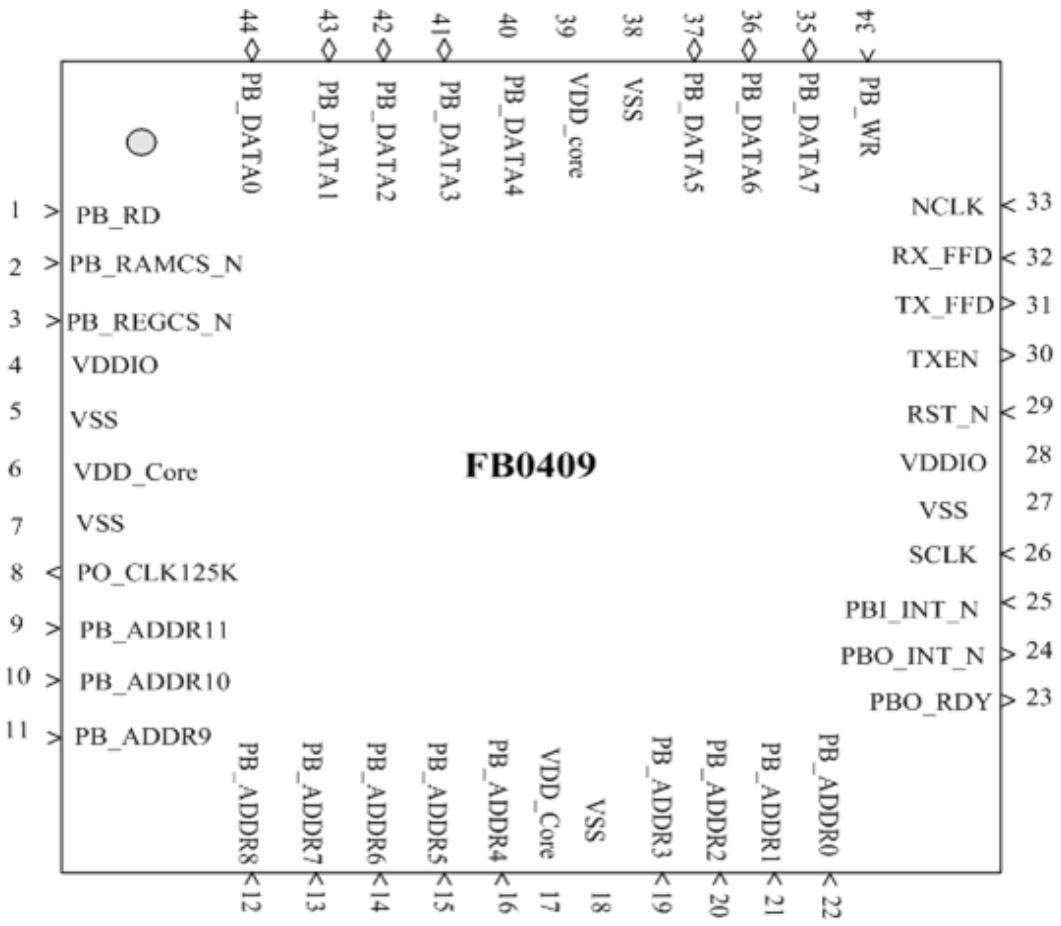


Figure 2 FBC0409 PIN Diagram

FBC0409 pins description

NAME	TYPE	Definition	Note
PB_ADDR[11:0]	INPUT	12 bits address bus	
PB_DATA[7:0]	INOUT	8 bits data bus	
PB_RAMCS_N	INPUT	internal RAM selection, active low	
PB_REGCS_N	INPUT	Register chip select, active low	
RST_N	INPUT	system reset, active low	
PB_WR	INPUT	CPU write control	
PB_RD	INPUT	CPU read control	
SCLK	INPUT	system clock, same source as CPU	
NCLK	INPUT	line clock, independent of SCLK	
PO_CLK125K	OUTPUT	125k time clock output	
PO_READY	OUTPUT	CPU delay request, PO_READY will active when	0 or hiZ

NAME	TYPE	Definition	Note
		CPU access internal SRAM which is busy	
PBO_INT_N	OUTPUT	interrupt request to CPU, active low	
PBI_INT_N	INPUT	interrupt input outside, active low	
TXEN	OUTPUT	FF Bus active indication, its level is decided by software	
TX_FFD	OUTPUT	FF Bus data output	
RX_FFD	INPUT	FF bus data input	
VDDIO	POWER	IO power, 3.3V or 5V	
VDD_CORE	POWER	core power, 3.3V	
VSS	GND	ground	

Table 2 FBC0409Pin description

6. Function Description

FBC0409 ff-bus controller conforms to IEC 61158 Filed Bus physical layer definition, and supports typical embedded CPU and MCU, such as Intel 80188/80186 serials and ARM. FBC0409 is satisfied in demands of high performance FF-Bus masters or slavers.

FBC0409 contains Manchester data encoder and decoder on chip. It requires only a medium interface and external filter for connection to a Foundation Field bus system, and automatically correct line polarity. FBC0409 also contains 4k build-in 8 bits data RAM, applying DMA controller. FF-Bus data receiving, transmitting and received address looking up are done without CPU intervening. Enough Rx and Tx process status is available in status registers of FBC0409, such as status of line operation, code error, frame loss, frame collision.

FBC0409 ff-bus controller realized a part of data-link layer function.: Tx/Rx frame check sequence (FCS), 16 bits 1MS timer, 16 bits 1/32MS timer, 16 bits octet timer, frame code decoding and address recognizing. These data link functions are designed to reduce the CPU time.

FBC0409 contains a timer for watchdog to avoid long time occupation on the FF bus line, when transmitting frame is longer than 512 bytes, the watchdog stops the transmitter. The built-in DMA controller manages three channels to access internal SRAM, which is able to enhance throughout and is friendly to software. The SRAM is 4k 8bits single port asynchronous SRAM, which is used as transmitting/receiving buffer and address table to filter input frame. Figure 3 is internal block diagram of FBC0409.

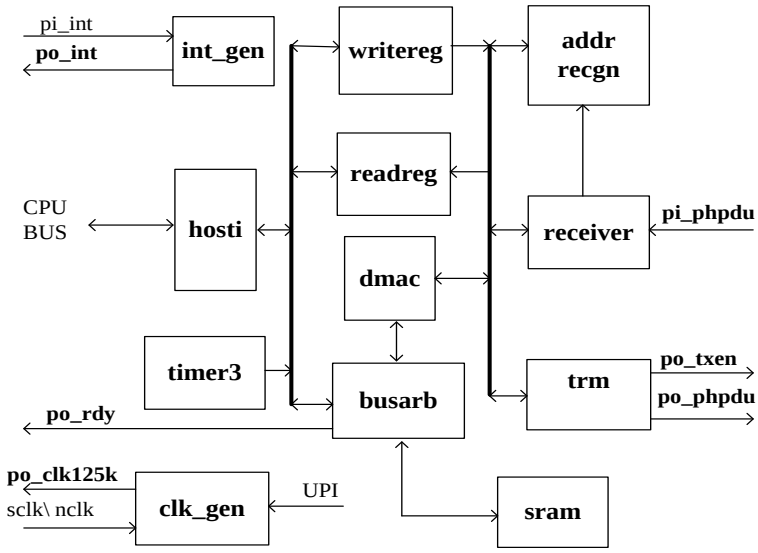


Figure 3 FBC0409 internal function block diagram

Note：The clock of bus arbiter and DMA/ interrupt controller is derived from SCLK, while in address recognization, bus data communication, timer, the 500KHZ clock is divided clock of SCLK or NCLK.

(1) CPU Interface

CPU interface block is bus interface between CPU and FBC0409, external CPU access registers and ram on FBC0409 through this block. Two access modes are supported, address sharing chip selection signal or address internal Register and RAM using different chip selection signals. Decode is done in this block according to chip selection signal and address bus to generate signals to operate internal RAM and registers.

Po_rdy is a shake-hand signal between CPU and FBC0409, when CPU accesses internal SRAM while the RAM bus is under control of internal function, po_rdy will be active to notice CPU to wait.

(2) Register function

This module is designed to receive configuration and command data from CPU or transmit internal data to CPU. CPU configures FBC0409 to operate correctly by accessing synchronously internal registers in this module. CPU writes or reads internal registers by asserting PB_REGCS_N signal active (share chip selection signals) , and, PB_WR active low when writes registers or PB_RD active low when reads registers .

(3) Timer

Timer is a counter based on internal 500k clock, which is divided by SCLK or NCLK, to provide three timers , 1 ms timer, 1/32 ms timer, octet timer(256 us),to data

link layer. All the three timers are 16 bits width and free running, and all are overflow to zero, accompanying a comparison value for each. Interrupts will be generated when any one of the three timers overflow or reach comparison value. Note that before CPU reads any one of these timers, write register 0x1f, which is used to latch timer value.

⑷ DMA Controller

DMA module is very important on FBC0409 that all the communication processes carry out automatically through this module after operation conditions are configured. DMA controller contains three channels, including receiving data storage (writing operation), transmitting data extraction (reading operation) and looking up address table (reading operation). This module generates bus signal interface to single port SRAM, at the same time, this module will give PO_READY active at CPU trying to access SRAM which is under control of DMA module.

⑸ Bus arbiter

Bus arbiter locates between DMA module and host interface to manage FBC0409 internal bus and external CPU bus requests to SRAM. DMA operation will wait until current CPU access finished, otherwise, PO_READY will be active at CPU access SRAM while DMA is controlling RAM bus. PO_READY will not be deserted whenever only DMA or only CPU access SRAM.

⑹ Address recognizing

This module is responsible for destination address filter in incoming frame by comparing destination address with internal stored node identifier or address table, then gives match indication and frame type information. Address comparing enabled after ARME bit in configure register is active, or else this module executes frame control word decoding only. Frame type information, including frame control word, broadcast frame, PSA frame and frame code, will obtain by frame decoding function. Additional, frame destination address type, node address, NS or HLNS address type will obtain, too. Address match performs according the type of destination address, if the address is node address, compare it with NODE_ID[7:0] directly and give notice AMOF to CPU; if the incoming destination address is HL or NS type， look up HL or NS address table in SRAM by DMA manner to compare and give AMOF or ETDF to CPU.

⑺ Bus receiver

Bus data receiver function focus on receiving incoming data from FF bus line and abstracts data sections to submit to up layers, including clock and data recovery, delimiter detection, Manchester decoding, serial to parallel transforming, FCS checking, and generates corresponding data and status. This module is configured by CPU to operate under receive enable control, under full or half duplex mode, under internal loop back operation.

This module can be configured in two receive mode, DMA manner or CPU

interrupt manner. In DMA manner (DRE is active) received data are stored into internal SRAM directly and are taken out after receive finishes. In CPU manner, the rx data full interrupt （RDRF_INT）will active after receive data register is full, then CPU responses this interrupt by taking out the register data. It is recommended to operate in DMA manner.

⑻ Bus transmitter

This module transmits the data delivered by CPU to FF bus by organizing frame structure, adding preamble and delimiter, performing parallel to serial and Manchester encoding, executing frame check. At the same time, generates corresponding status and interrupt signals to CPU. CPU controls the operation of bus transmitter, including enable the module to work, preamble length configuration, transmitting frame CRC enable. Similar to receiver, the transmitter also has two manners in operation, DMA mode and CPU mode. When DMA enable (DTE) is active, the transmitting data block is written into internal SRAM and data length has been configured before initialize transmitting by DMA controller. In CPU manner, initialize transmitter first, then do nothing until transmit register empty interrupt signal (TDRE_INT) is active to request next byte to be transmitted. After all byte have been transmitted, transmitter stops. It is recommended to operate in DMA manner.

Note that transmit register（TRM_REG）must be executed a idle writing to start process of transmit. There are two mechanism to notify CPU to finish current transmitting, one is transmitting byte counter in transmitter is reach configure number, other is that timer is more than one byte time without data to write in transmitter. The transmitter build in watchdog timer to avoid transmit Jabber, at once the transmitting byte number get to 512, transmitter stops and give Jabber interrupt indication JI_INT to CPU.

⑼ Clock generator

This module generates the required clocks of internal function blocks, including 500 KHz clock used in transmitter and receiver, fast clock used in DMA controller and bus arbiter. If clock mode is enabled (MD[1:0]≠00), internal fast clock SCLK is decided by system clock divider CLK_DIV, formula is SCLK/（CLK_DIV +1）. According to time constraints of internal asynchronous SRAM access, the generated clock must not be faster than 8MHz, if input clock is 32MHZ, thus the value of CLK_DIV should be more than 0x3; if input clock is 20MHZ, CLK_DIV should be more than 0x1. Note that divider must be one of 1/2/4/8/16 （CLK_DIV equal to 0/1/3/7/15）.The 500KHz clock is decided by SCLK, NCLK and command register 2. CLKSEL selects source clock, 0 is SCLK, 1 is NCLK, then divided by BR [4:0] to obtain 500KHz clock.

MD definition：00: clock stops,01:H1 bit rate, it is no effect of other value.

BR definition：CLK500 =ICLK/(BR+1), BR is one of 0/1/3/7/15/31.

⑽ Interrupt function

This module generates interrupt signals through internal status signals, and

executes interrupt clearing, interrupt masking. Note that when writing 1 to the corresponding bit of interrupt address, the interrupt will be cleaned. Masking interrupt also clears it, and the interrupt bit will never generate until the mask bit convert to 1. Note that the interrupt cleaning operation is executed on interrupt address.

7. Address mapping

The address space of FBC0409 can be divided into two parts, register area and 4k ram area, depending on addressing mode and MSB of address bus. Two method of addressing is supported in FBC0409 based on chip selection signal connection. One is that only one chip select is connected to both pins of REG_CSN and RAM_CSN, another is that pin of REG_CSN connects to pin of CS_n of CPU and RAM_CSN connects to CS_m of CPU. Here we call the former method 1 and the latter method 2.

In method 2, separate address corresponds to register space and ram space; in this manner address decoding performs independently according to chip selection signal of each other. When register chip selection is active, at this time ram chip selection is deserted, the address of register is between 6'H00 and 6'H3F. When ram chip selection is active, at this time register chip selection is deserted, the address of ram is between 12'H000 and12'HFFF.

In method 1, address space is shared between register area and ram area, that is register space is between 12'HFC0 and 12'HFFF, ram space is between 12'H000 and 12'HFBF. It is recommended to use independent addressing method, method 2.

8. FBC0409 Register

FBC0409 Register。

Offset	Name	Description	Attribute	Note
0x00	TRM_REG[7:0]	transmit data register	WO	DATA REG
	RCV_REG[7:0]	receive data register	RO	
0x01	FB_CMD0[5:0]		W/R	CMD REG
	PSE[1:0]	0x01[1:0]，preamble length		
	TFCE	0x01[2]，transmit FCS enable		
	TDE	0x01[3]，transmit data enable		
	FDM	0x01[4]，duplex enable		
	RDE	0x01[5]，Rx data enable		
0x02	FB_CMD1[4:0]		W/R	CMD REG
	ARME	0x02[0]，address recognize mode enable		
	DRE	0x02[1]，DMA Rx enable		
	DTE	0x02[2]，DMA Tx enable		

Offset	Name	Description	Attribute	Note
	LOOPBK	0x02[3]，Loop back control		
	MAU_ENF	0x02[4]，MAU Tx enable flag		
0x03	FB_CMD2[7:0]		WO	CMD REG
	BR[4:0]	0x03[4:0], clock division scaler, obtain 500K clock		
	MD[1:0]	0x03[6:5],time mode, 00：silent		
	CLKSEL	0x03[7], clock select control		
0x03	ISR_MSTR[4:0]		RO	INTERRUPT MASTER
	CISF	0x03[0], indicates communication interruption		
	AISF	0x03[1] , indicates address recognizeation interruption		
	TISF	0x03[2], indicates TIMER/ CLOCK interruption		
	ERRF	0x03[3]，indicates error		
	EIF	0x03[7]，PI_INT is int		
0x04	ISR0[7:0]		RC	INT0
	TDRE_INT	0x04[0]，tx register blank		
	TIF_INT	0x04[1]，data tx finish		
	RIF_INT	0x04[2]，data rx finish		
	REDF_INT	0x04[3],receive end delimiter		
	REF_INT	0x04[4], rx register overflow		
	RSDF_INT	0x04[5],receive start delimiter		
	RAF_INT	0x04[6]，FF bus active		
	RDRF_INT	0x04[7]，rx register full		
0x04	INT_CLR0[7:0]	writing 1 to clear corresponding interruption	WO	CLEAR INT0
0x05	ISR1[3:0]		RC	INT1
	BMDF_INT	0x05[0]，rx broadcast		
	AMDF_INT	0x05[1]，rx address match		
	EOTF_INT	0x05[2]，address table look up finish		
	FCF_INT	0x05[3]，recognize address code		
0x05	INT_CLR1[3:0]	writing 1 to clear corresponding interruption	WO	CLEAR INT1
0x06	ISR2[5:0]		RC	INT2
	MS1_32COF_INT	0x06[0], 1/32MS timer overflow		
	MS1_32CF_INT	0x06[1]，1/32MS timer reach to comp value		
	MS1COF_INT	0x06[2]，1MS timer overflow		
	MS1CF_INT	0x06[3]，1MS timer reach to comp		

Offset	Name	Description	Attribute	Note
		value		
	OOF_INT	0x06[4]，timer overflow		
	OCF_INT	0x06[5]，timer reach to comp value		
0x06	INT_CLR2[5:0]	corresponding interrupt cleaned by writing 1	WO	CLEAR INT2
0x07	ISR3[6:0]		RC	INT3
	LSDF_INT	0x07[0], rx start delimiter		
	LEDF_INT	0x07[1], rx end delimiter		
	LNGFRM_INT	0x07[2] rx slong frame		
	MDERR_INT	0x07[3] rx Manchester code		
	LCD_INT	0x07[4],loss CD when recieving		
	TRM_FAIL_INT	0x07[5], transmit failure		
	JI_INT	0x07[6],jibber indication		
0x07	INT_CLR3[6:0]	clean corresponding interrupt by writing 1	WO	CLEAR INT3
0x08	ISR0_MSK[7:0]	mask of ISR0	W/R	
0x09	ISR1_MSK[3:0]	mask of ISR1	W/R	
0x0A	ISR2_MSK[5:0]	mask of ISR2	W/R	
0x0B	ISR3_MSK[6:0]	mask of ISR3	W/R	
0x0C	TRM_BYTECNT[13:8]	MSB of Tx bytes counter	W/R	
0x0D	TRM_BYTECNT[7:0]	LSB of Tx bytes counter	W/R	
0x0E	TRM_BUFPTR[13:8]	MSB of tx data buffer pointer when in DMA mode	W/R	
0x0F	TRM_BUFPTR[7:0]	LSB of tx data buffer pointer when in DMA mode	W/R	
0x10	reserved	used in the future		
0x11	reserved	used in the future		
0x12	RCV_BUFPTR[13:8]	MSB of Rx data buffer pointer when in DMA mode	W/R	
0x13	RCV_BUFPTR[7:0]	LSB of Rx data buffer pointer when in DMA mode	W/R	
0x14	reserved	used in the future		
0x15	reserved	used in the future		
0x16	MATCH_VECT[13:8]	MSB of address match vector	RO	
0x17	MATCH_VECT[7:0]	LSB of address match vector	RO	
0x16	ADR_TABNS[13:8]	MSB of NS table pointer	WO	
0x17	ADR_TABNS[7:0]	LSB of NS table pointer	WO	
0x18	FRAME_CODE[4:0]	frame code received	RO	
0x19	FRAME_CONTRL[7:0]	frame control code received	RO	
0x18	ADR_TABHLNS[13:8]	MSB of HLNS table pointer	WO	CONFIGURE
0x19	ADR_TABHLNS[7:0]	LSB of HLNS table pointer	WO	CONFIGURE

Offset	Name	Description	Attribute	Note
0x1A	reserved	used in the future		
0x1B	NODE_ID[7:0]	node identifier address	W/R	CONFIGURE
0x1C	STATUS0[7:0]		RO	STATUS0
	TDRE_STAT	0x1C[0]，Tx register blank		
	TIF_STAT	0x1C[1]，data Tx finish 示		
	FCSF__STAT	0x1C[2]，FCS correct		
	REDF_STAT	0x1C[3]，receive data end delimiter		
	RDEF_STAT	0x1C[4]，receive buffer overflow		
	RSDF_ STAT	0x1C[5]，receive data start delimiter		
	RAF_ STAT	0x1C[6]，FF Bus active		
	RDRF_STAT	0x1C[7]，Rx register is full		
0x1D	STATUS1[7:0]		RO	STATUS1
	RBMF_STAT	0x1D[0] ，broadcast address recognized		
	AMOF_STAT	0x1D[1]，address match flag		
	ETDF_STAT	0x1D[2]，table lookup end		
	RFCF_STAT	0x1D[3]，frame control code received		
	RPSAF_STAT	0x1D[4]， PSA frame received		
	RNAF_STAT	0x1D[5]，node address received（8bit address）		
	NS_STAT	0x1D[6]，NS address request(16bits)		
	HL_STAT	0x1D[7]，HL address request (32bits adderss)		
0x1E	STATUS2[6:0]		RO	STATUS2
	LSDF_STAT	0x1E[0],loss of start delimiter error		
	LEDF_STAT	0x1E[1],loss of end delimiter		
	LNGFRM_STAT	0x1E[2]，long frame reeived		
	MDERR_STAT	0x1E[3], Manchester code error		
	LCD_STAT	0x1E[4]，loss carrier when receiving		
	LTAF_STAT	0x1E[6] ，address table lookup requesting		
	RSPF_STAT	0x1E[7],disparity indication		
0x1F	TIMER_LATCH	latch timer control, active when write 0xff		
0x20	MS1_32CNT[15:8]	1/32MS timer MSB	RO	
0x21	MS1_32CNT[7:0]	1/32MS timer LSB	RO	
0x20	MS1_32COMP[15:8]	1/32MS comp value MSB	WO	
0x21	MS1_32COMP[7:0]	1/32MS comp value LSB	WO	
0x22	MS1_CNT[15:8]	1MS timer MSB	RO	
0x23	MS1_CNT[7:0]	1MS timer LSB	RO	
0x22	MS1_COMP[15:8]	1MS comp value MSB	WO	

Offset	Name	Description	Attribute	Note
0x23	MS1_COMP[7:0]	1MS comp value LSB	WO	
0x24	OCT_CNT[15:8]	Octet timer MSB	RO	
0x25	OCT_CNT[7:0]	Octet timer LSB	RO	
0x24	OCT_COMP [15:8]	Octet comp value MSB	WO	
0x25	OCT_COMP [7:0]	Octet comp value LSB	WO	
0x26	CLK_DIV [3:0]	RAM write/read pulse width control	WR	
0x27	test	fix value of 0x01	W/R	

Table 3 FBC0409Register list

Divide registers into eight groups according different function：transmitting Registers, receiving Registers, Command Registers, interruption Registers, DMA control Registers, Address recognization Registers and timer registers, as show as below.

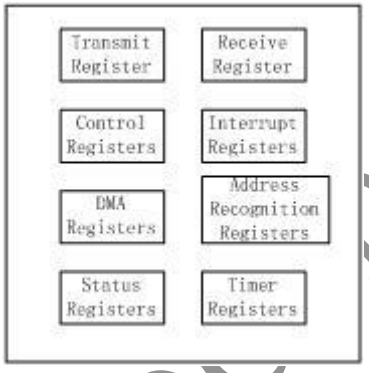


Figure 4 FBC0409 internal Register group

transmit data register（TRM_REG）——address 0x00

FBC0409 is designated two modes sending data to FF bus, which is CPU manner and DMA manner. CPU transmits data directly through writing transmit data register which address is 0x00. In order to avoid transmit data overflow and prepare transmit module, the CPU should read the status bit of TDRE (status Regiter0, address 0x1c, bit[0]) or interrupt status TDRE_INT (Interrupt status Register0,adderss 0x04, bit 0) first, if TDRE or TDRE_INT is true，which indicates that the transmit data register is blank, now new data should be written and clear the current interrupt to wait for next byte to transmit. All steps above are automatically performed in DMA manner when transmit data has been stored in Tx buffer and transmit has been initialized.

Additional, initialization is done by writing transmit data register in all two mentioned manners. When writing to transmit data register in idle state, the first operation is deemed start the transmittion, the data should be ignored, the valid data follows. And, it is no effects to write transmit data register in DMA mode.

receive data register(RCV_REG)**——address 0x00**

The receive data register stores data received from FF bus and is accessed by CPU when reading address 0x00. Similarly to transmit data register, in order to avoid this register under run (Cause Frame error) or overflow (loss of frame data), CPU should read status register RDRF（status register0，address 0x1C, bit 1） or interrupt

status register RDRF_INT（interrupt status register，address 0x04,bit 1）, and if RDRF or RDRF_INT is true，which indicates one new byte data has been received, CPU read the data immediately. In the DMA manner, all the steps automatically performed, receive data is store in the SRAM on chip.

Command Registers

Command registers decide FBC0409 operation configuration and common control, including three command registers. Here is detail.

Command Register0（FB_CMD0）——address 0x01

0	0	RDE	FDM	TDE	TFCE	PSE[1:0]

RDE—RECEIVE DATA ENABLE: ff bus data receive control, 0 disable receive, 1enable receive.

FDM—FULL/HALF DUPLEX MODE: full duplex/half duplex mode selection, 1 full duplex ,0 half duplex.

TDE—TRANSMIT DATA ENABLE: ff bus data transmit control, 0 disable transmit, 1enable transmit.

TFCE—TRANSMIT FRAME CHECK ENABLE: Transmit FCS enable, 0 disable FCS; 1,FCS enable.

PSE[1:0]—PREAMBLE SEQUENCE ENABLE: preamble length configure, 00：1byte,01：2 bytes,10：3 bytes,11：4 bytes.

Command Register 1（FB_CMD1）——address 0x02

0	0	0	MAU_ENF	LOOPBK	DTE	DRE	ARME

MAU_ENF—MAU ENABLE FLAG: MAU enable flag，transmit enable to MAU is high level when transmit active setting this bit to 1, otherwise, set this bit to 0

LOOPBK—LOOPBACK MODE FLAG: Internal loop back control, transmit will internal loop back when set this bit to 1.

DTE—DMA TRANSMIT ENABLE : DMA transmit enable control, 0：disable DMA transmit, 1：enable DMA transmit

DRE—DMA RECEIVE ENABLE: Enable DMA receive, 0：disable DMA receive, 1：Enables DMA receive

ARME—ADDRESS RECOGNITION MODE ENABLE: Enable address recognize mode, effect when 1

Command Register 2（FB_CMD2）——Address 0x03

CLKSEL	MD1	MD0	BR4	BR3	BR2	BR1	BR0

CLKSEL—CLOCK SOURCE SELECTS : line clock source selects, 0：CPU clock SCLK，1：NCLK

MD1-MD0—CLOCK MODE SELECTS , disable internal clock when is set to 2’b11, otherwise configure ff bus communication rate 31.25KHZ.

BR[4:0]—BAUD RATE SELECT , divider to get the internal 500kHz clock used the clock select by CLKSEL, formula: input clock/（BR+1）. E.g. input clock is 16MHZ， thus BR4-BR0should be 0x1f. This value only supports

1/2/4/8/16/32 division, corresponding BR is 0/1/3/7/15/31.

Command Register 3（FB_CMD3）——Address 0x26

0	0	0	0	CLK_DIV[3:0]

CLK_DIV[3:0]—internal clock divider, get 4~6M clock by divides SCLK using SCLK/（CLK_DIV +1）. E.g. if input clock is 32MHZ,thus the value of CLK_DIV should be 0x7; if input clock is 20MHZ, thus CLK_DIV should be 0x3. Only 1/2/4/8/16 supported , (CLK_DIV is 0/1/3/7/15).

Interrupt Registers

Several interrupt provided on FBC0409, including interrupt index Register, interrupt status register0-3, interrupt mask regiter0-3.

Interrupt Index Register（ISR_MSTR）——Address 0x03

Interrupt index register indicates the source of interrupt

EIF	0	0	0	ERRF	TISF	AISF	CISF

EIF—EXTERNAL INTERRUPT FLAG, outside interrupt indication，active when PI_INT ＝0.

ERRF—interrupt caused by error. Any bit in ISR3 is high this bit is active (high).

TISF—TIMER INTERRUPT SOURCE FLAG, Any bit of six in ISR2 is high this bit is active (high).

AISF—ADDRESS INTERRUPT SOURCE FLAG. Any bit of four in ISR1 is high AISF active (high).

CISF—COMMUNICATION INTERRUPT SOURCE FLAG . Any bit of eight in ISR0 is high CISF active (high).

Note：Any bit of four in ISR_MSTR is 1, output pin PO_INT is active low.

Interrupt status Register0（ISR0）——Address 0x04

Interrupt status register0 stores the interrupts generated in communication process and are cleaned by writing 1 to corresponding bit at the same address.

RDRF_INT	RAF_INT	RSDF_INT	REF_INT	REDF_INT	RIF_INT	TIF_INT	TDRE_INT

RDRF_INT—RECEIVE DATA REGISTER FULL . RDRF_INT is active high when receive module has received one whole byte.

RAF_INT—RECEIVE ACTIVE FLAG . RAF_INT is active high when detects the CD signal on line.

RSDF_INT—RECEIVE START DELIMITER FLAG. RSDF_INT is active high when Start delimiter is detected.

REF_INT—RECEIVE ERROR FLAG. REF_INT is active high when receive data Register overflows.

REDF_INT—RECEIVE END DELIMITER FLAG. REDF_INT is active high after detecting frame end delimiter, it also indicates the current receive finished.

RIF_INT—RECEIVE IDLE FLAG . RIF_INT is active high after frame receives finish.

TIF_INT—TRANSMIT IDLE FLAG. TIF_INT is active high after frame transmits finish, and indicates another frame can be initialized.

TDRE_INT－TRANSMIT DATA REGISTER EMPTY. TDRE_INT is active high when transmit module requests a new byte to transmit

Interrupt status Register 1（ISR1）——Address 0x05

Interrupt status register1 stores interrupt status caused in address recognize processes and are cleaned by writing 1 to corresponding bit at the same address.

0	0	0	0	FCF_INT	EOTF_ING	AMDF_INT	BMDF_INT

FCF_INT－FRAME CONTROL FLAG . FCF_INT is active high when frame control word is received in address recognize module.

EOTF_INT－END OF TABLE FLAG. ETOF_INT is active high when lookup table gets to the end（continuous 0 address）.

AMDF_INT－ADDRESS MATCH DETECTION FLAG. AMDF_INT is active high when address matches.

BMDF_INT－BROADCAST MESSAGE DETECTION FLAG . BMDF_INT=1 when Current receiving frame is a broadcast frame.

Interrupt status Register 2（ISR2）——Address 0x06

Interrupt status register2 stores interrupt status caused in timer module and are cleaned by writing 1 to corresponding bit at the same address.

0	0	OCF	OOF	1CF	1OF	1/32CF	1/32OF

OCF－OCTET COUNTER FLAG . Octet timer gets to comp value interrupt. OCF is active high. Note: The timer and the comp value are all 0 when RESET, this bit will active after reset, clean it before use。

OOF－OCTET OVERFLOW FLAG. Octet timer overflow interrupt (get to 0xFFFF), OOF is active high.

1CF－1MS COUNTER FLAG. 1MS timer gets to its comp value, same as OCF.

1OF－1MS OVERFLOW FLAG. 1Ms timer overflow interrupt indication, same as OOF.

1/32CF－1/32MS COUNTER FLAG. 1/32MS timer gets to comp value, same as OCF.

1/32OF－1/32MS OVERFLOW FLAG . 1/32MS overflow interrupt.

Interrupt status Register 3（ISR3）——Address 0x07

Interrupt status register3 stores interrupt caused by error status and are cleaned by writing 1 to corresponding bit at the same address.

0	JI_INT	TRM_FAIL_INT	LCD_INT	LNGFRM_INT	MDERR_INT	LEDF_INT	LSDF_INT

JI_INT－JABBER INDICATION . Active high when jibber happened.

TRM_FAI_INT－TRANSMIT FAILUE . Active high when transmit was initialized without data.

LCD_INT－LOST CARRIER DETECTION. Loss of carrier in processing of receiving. Active high.

LNGFRM_INT－LONG FRAME. Long frame input error interrupt, active high.

MDERR_INT－MANCHESTER DECODE ERROR. Code error in input Manchester code stream, active high.

LEDF_INT－LOST END DELIMITER FLAG. Loss of frame end delimiter when receiving, active high.

LSDF_INT－LOST START DELIMITER FLAG. Loss of start delimiter in receive process.

Interrupt0 mask Register（ISR0_MSK）——Address 0x08

Interrupt mask register0 is used to disable or enable corresponding interrupt bit. Interrupt bit is enabled by setting mask bit to 1, otherwise clear it.

Interrupt1 mask Register（ISR1_MSK）——Address 0x09

Interrupt mask register1 is used to disable or enable corresponding interrupt bit. Interrupt bit is enabled by setting mask bit to 1, otherwise clear it.

Interrupt2 mask Register 2（ISR2_MSK）——Address 0x0A

Interrupt mask register2 is used to disable or enable corresponding interrupt bit. Interrupt bit is enabled by setting mask bit to 1, otherwise clear it.

Interrupt3 mask Register（ISR3_MSK）——Address 0x0B

Interrupt mask register3 is used to disable or enable corresponding interrupt bit. Interrupt bit is enabled by setting mask bit to 1, otherwise clear it.

Configure Registers

Transmit Bytes counter Register（TRM_BYTECNT[13:0]）——Address 0x0C-0x0D

Transmit byte number configure in DAM mode. Write MSB first, followed by LSB immediately when change the configuration.

Transmit buffer pointer Register（TRM_BUFPTR[13:0]）——Address 0x0E-0x0F

Transmit buffer pointer in DMA mode. Write MSB first, followed by LSB immediately when change the Register.

Receive buffer pointer Register（RCV_BUFPTR[13:0]）——Address 0x12-0x13

Receive data buffer pointer, points to current frame storage start address in SRAM in DMA mode, and indicates the current frame end address minus 1. Write MSB first, followed by LSB immediately when change the Register.

Address match vector Register（MATCH_VECTOR[13:0]）——Address 0x16-0x17

Points to the next address after operation of address recognization whenever match or not. Read only.

NS Address table pointer Register（ADR_TABNS[13:0]）——Address 0x16-0x17

The start address of NS address-table in SRAM， Write only. Write MSB first, followed by LSB immediately when changing the Register.

Frame control word Register (FRAME_CNTRL[7:0]) ——Address 0x18

Store the frame control word in received FF bus data, read only.

Frame code Register (RAME_CODE[4:0]) ——Address 0x19

Stores the decode information of frame control word, 5 bits. CPU can access it after frame control word indication is active. Encoding rules lists in table 3.

FCODE	MESSAGE FUNCTION	FCODE	MESSAGE FUNCTION
00000	ESTABLISH CONNECTION 1	10000	DATA TRANSFER 5
00001	ESTABLISH CONNECTION 2	10001	STATUS RESPONSE
00010	DISCONNECT CONNECTION 1	10010	COMPEL TIME
00011	DISCONNECT CONNECTION 2	10011	TIME DISTRIBUTION
00100	RESET CONNECTION 1	10100	ROUND-TRIP QUERY
00101	RESET CONNECTION 2	10101	ROUND-TRIP REPLY
00110	COMPEL ACKNOWLEDGE 1	10110	PROBE NODE
00111	COMPEL ACKNOWLEDGE 2	10111	PROBE RESPONSE
01000	COMPEL DATA 1	11000	PASS TOKEN
01001	COMPEL DATA 2	11001	EXECUTE SEQUENCE
01010	EXCHANGE DATA 1	11010	RETURN TOKEN
01011	EXCHANGE DATA 2	11011	REQUEST INTERVAL
01100	DATA TRANSFER 1	11100	CLAIM LAS
01101	DATA TRANSFER 2	11101	TRANSFER LAS
01110	DATA TRANSFER 3	11110	WAKE UP
01111	DATA TRANSFER 4	11111	IDLE

Table 4 frame code/frame type table

HLNS address table pointer Register(ADR_TABHLNS[13:0]）——Address 0x18-0x19

The start address of HLNS address lookup table in SRAM，Write only. Write MSB first, followed by LSB immediately when changing the Register. If input frame is of HLNS type address, this table is used to match destination address.

Node Identifier Register（NODE_ID）——Address 0x1B

Store 8 bits node identifier.

Status Registers

Status Register0（STATUS0）——Address 0x1C

Status register0 stores the status information in communication process. Read only.

RDRF_STAT	RAF_STAT	RSDF_STAT	REF_STAT	REDF_STAT	FCSF_STAT	TIF_STAT	TDRE_STAT

RDRF_STAT—RECEIVE DATA REGISTER FULL .RDRF_STAT is active high when receive module has received one whole byte.

RAF_STAT—RECEIVE ACTIVE FLAG. RAF_STAT is active high when detects the CD signal on line.

RSDF_STAT—RECEIVE START DELIMITER FLAG. RSDF_STAT is active high when Start delimiter is detected

REF_STAT—RECEIVE ERROR FLAG. REF_STAT is active high when receive data Register

overflows.

REDF_STAT—RECEIVE END DELIMITER FLAG. REDF_STAT is active high after detects frame end delimiter; it also indicates the current receive finished.

FCSF_STAT—FRAME CHECK SEQUENCE FLAG. RIF_STAT is active high when Rx FCS is error.

TIF_STAT—TRANSMIT IDLE FLAG. TIF_STAT T is active high after frame transmits finish, and indicates another frame can be initialized.

TDRE_STAT—TRANSMIT DATA REGISTER EMPTY. TDRE_STAT is active high when transmit module request new byte to transmit

Status Register 1（STATUS1）——Address 0x1D

Status register1 stores the status information in address recognition process. Read only.

HL_STAT	NS_STAT	RNAF_STAT	RPSAF_STAT	RFCF_STAT	ETDF_STAT	AMOF_STAT	RBMF_STAT

HL_STAT—HIGH LINK FLAG. HLNS_STAT is active high when HL address frame received

NS_STAT—NODE SELECT FLAG. NS_STAT is active high when NS address frame received

RNAF_STAT—RECEIVE NODE ADDRESS FLAG. Active when NODE ID address frame received

RPSAF_STAT—RECEIVE PSA FLAG. Active when PSA frame received

RFCF_STAT—RECEIVE FRAME CONTROL FLAG. FCF_STAT is active high when frame control word is received in address recognize module.

ETDF_STAT—END OF TABLE DETECTION FLAG . ETOF_STAT is active high when lookup table get to the end（continuous 0 address）.

AMOF_STAT—ADDRESS MATCH OCCURENCE FLAG . AMDF_STAT is active high when address matches.

RBMF_STAT—RECEIVE BROADCAST MESSAGE FLAG. BMDF_STAT when Current receiving frame is a broadcast frame.

Status Register 2（STATUS2）——Address 0x1E

Status register2 stores the error status information. Read only.

RSPF_STAT	LTAF_STAT	0	LCD_STAT	MDERR_STAT	LNGFRM_STAT	LEDF_STAT	LSDF_STAT

RSPF_STAT—REVERSED SIGNAL POLARITY FLAG. Disparity indication.

LTAF_STAT—LOOKUP TABLE ACTIVITY FLAG. Address table lookup is in process。

LCD_STAT—LOST CARRIER DETECTION. LCD_STAT is active when loss of carrier in processing of receives. Active high.

LNGFRM_STAT—LONG FRAME. LNGFRM_STAT is active when long frame input error happened. Active high.

MDERR_STAT—MANCHESTER DECODE ERROR. MDERR_STAT is active when code error in input Manchester code stream. Active high.

LEDF_STAT—LOST END DELIMITER FLAG. LEDF_STAT is active when loss of frame end delimiter when receiving. Active high。

LSDF_STAT—LOST START DELIMITER FLAG. LSDF_STAT is active when loss of start

delimiter in receive processes.

Timer Registers

Timer Registers latch control (TIMER_LATCH)**——Address 0x1f**

Issue writing operation of this register first before get the internal timer, used to latch internal timer.

1/32MS timer Register（MS1_32CNT[15:0）——Address 0x20-0x21

1/32MS timer register, read only

1/32MS timer comp value（MS1_32COMP[15:0]）——Address 0x20-0x21

1/32MS timer comparison value, write only.

1MS timer Register（MS1_CNT[15:0]）——Address 0x22-0x23

1MS timer register, read only

1MS timer comp value (MS1_COMP[15:0]）——Address 0x22-0x23

1MS timer comparison value, write only.

Octet timer Register（OCTET_CNT[15:0]）——Address 0x24-0x25

Octet timer register, read only

Octet timer comp value (TET_COMP[15:0]）——Address 0x24-0x25

Octet timer comparison value, write only.

9. Package information

FBC0409 is a TQFP44package.

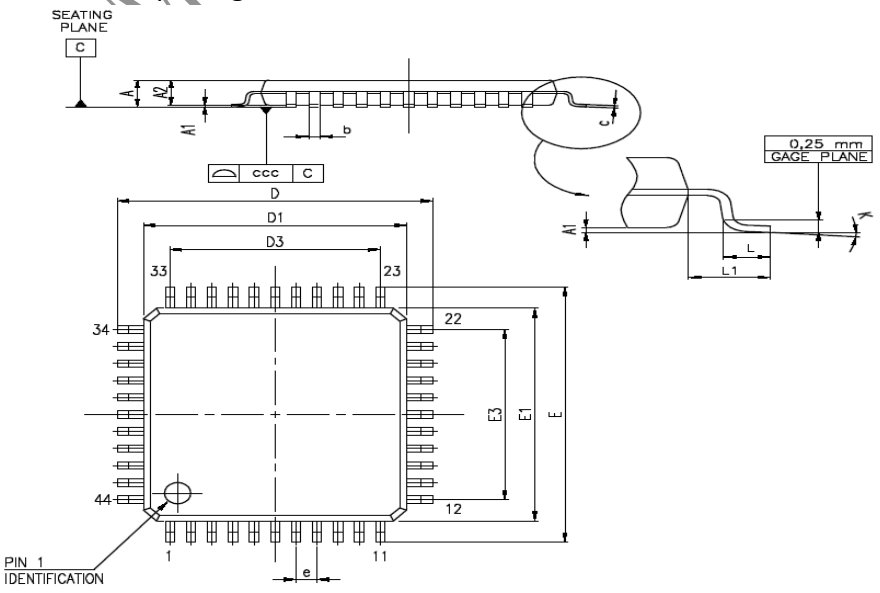


Figure 5 Package diagram

Package

DIMENSIONS						
REF.	**mm**			**Inch**		
	MIN.	**TYP.**	**MAX**	**MIN.**	**TYP.**	**MAX**
A			1.6			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.45	0.012	0.015	0.018
C	0.09		0.20	0.004		0.008
D	11.80	12.00	12.20	0.465	0.472	0.480
D1	9.8	10.00	10.20	0.386	0.394	0.402
D3		8.00			0.315	
E	11.80	12.00	12.20	0.465	0.472	0.480
E1	9.80	10.00	10.20	0.386	0.394	0.402
E3		8.00			0.315	
E		0.80			0.031	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0°	3.5°	7°	0°	3.5°	7°

Table 5 Packages information

10.Characteristics

(1) Thermal Information

- ✧ Storage temperature：-65~150℃；
- ✧ Operating temperature：-40~85℃；
- ✧ long-term operating junction temperature：-40~85℃

(2) D.C/A.C. characteristics

D.C. characteristics

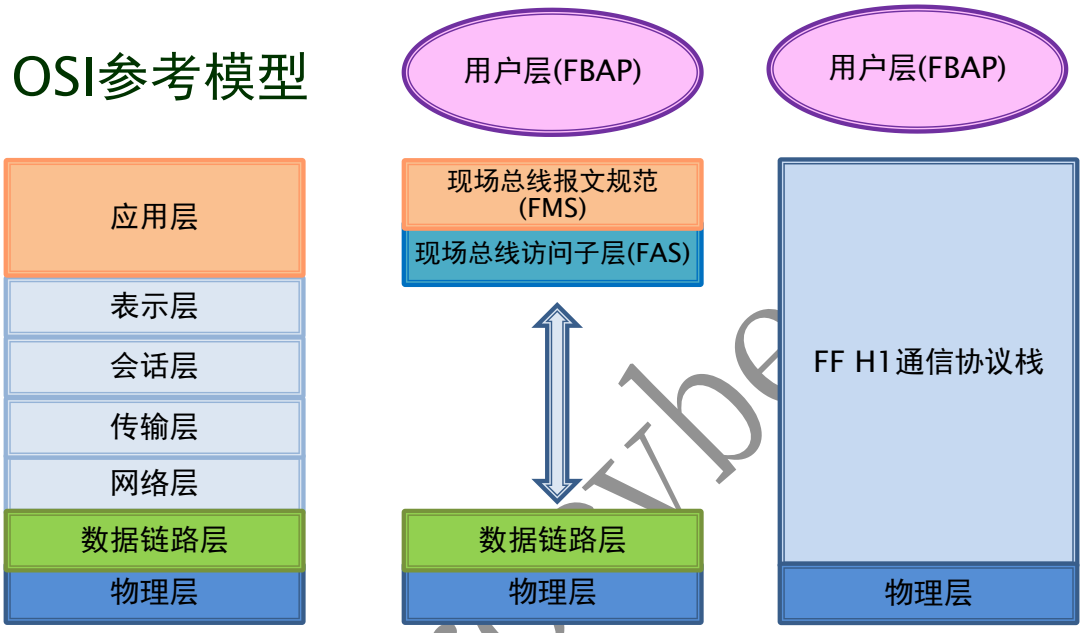
SYMBOL	PARAMETER	OP CONDATIONS	MIN	TYP	MAX	UNIT
VDD	PRE-SUPPLY VOLTAGE		3.0	3.3	3.60	V
VDDCORE	DC SUPPLY IO/CORE		3.0	3.3	3.60	V
VIH	INPUT HI-VOLTAGE		2.0		5.5	V
VIL	INPUT LO-VOLTAGE		-0.3		0.8	V
VT	THRESHOLD POINT		1.29	1.37	1.47	V
VT+	SCHMITT TRIG. LOW TO HI THRESHOLD	RST_N	1.51	1.58	1.64	V
VT-	SCHMITT TRIG. HI TO LOW THRESHOLD	RST_N	0.93	0.98	1.03	V
VOH	OUTPUT HI-VOLTAGE	@IOH=2,4,…24MA	2.4			V
VOL	OUTPUT LO-VOLTAGE	@IOL=2,4,…24MA			0.4	V
IL	INPUT LEAK-CURRENT				±10	UA
IOZ	3-STATE OUTPUT LEAKAGE-CURRENT				±10	UA
RPU	PULL-UP RESISTOR		33	45	74	KOHM
RPD	PULL-DOWN RESISTOR		33	45	74	KOHM
IOH	HIGH LEVEL OUTPUT CURRENT @VOH=2.4V	2MA				
IOH	LOW LEVEL OUTPUT CURRENT @VOL=0.4V	2MA				

Table 6 FBC0409D.C. characteristics

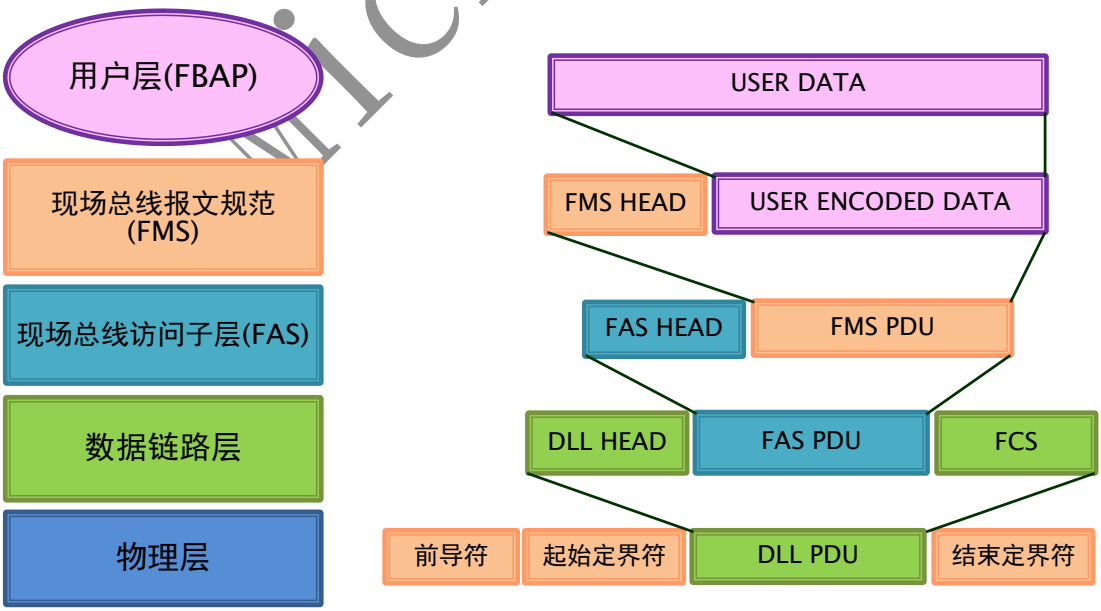
附录二 FF 总线技术，标准及规范简介

1. 通信协议

- OSI 参考模型



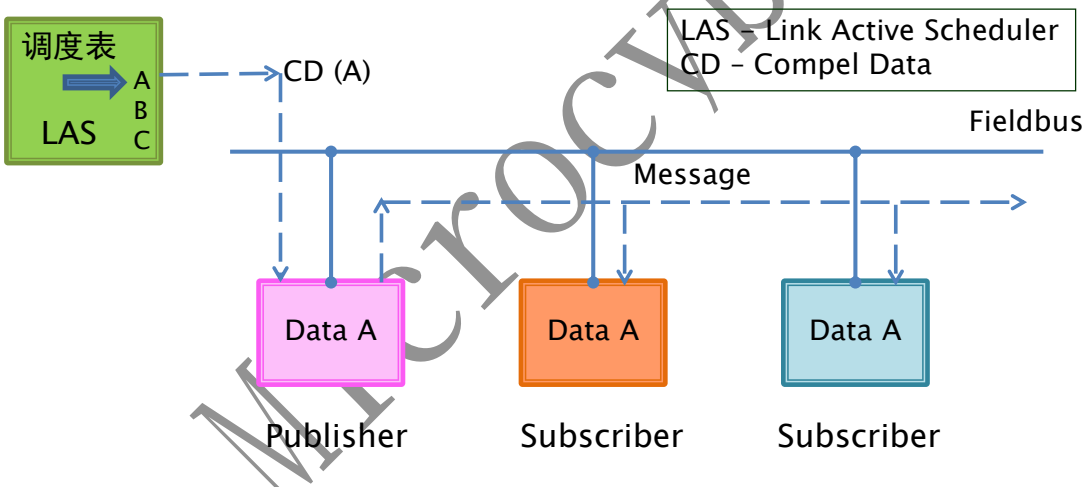
- FF 报文结构



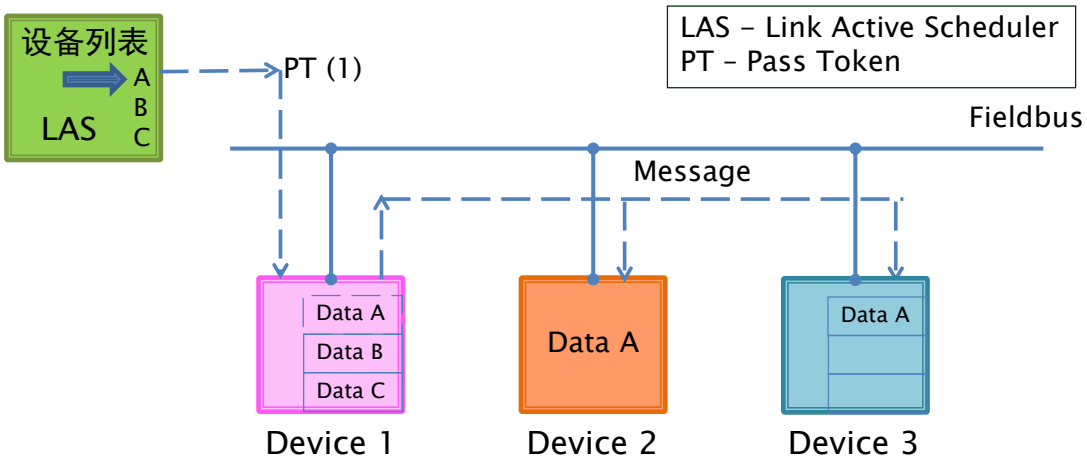
- 链路活动调度器”（LAS）控制总线通信
  - 系统时钟发布

- 网络通信调度
- 设备列表维护
- 支持冗余

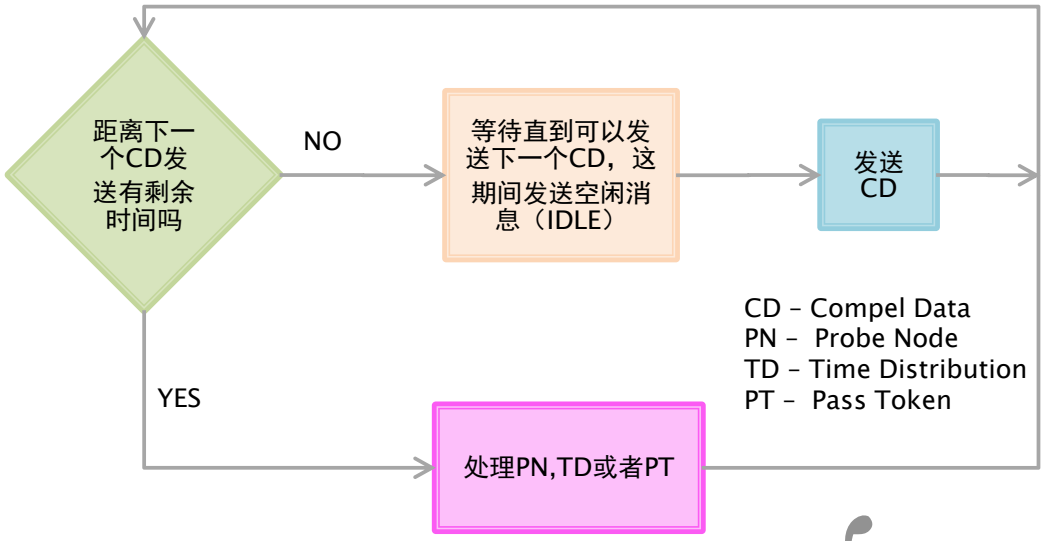
- 设备类型
  - 链路主设备（Link Master）- 有能力支持 LAS 功能
  - 基本设备（Basic）- 没有能力支持 LAS 功能
  - 网桥设备（Linking Device）- 将单个现场总线网段组合链接在一起
- 设备 ID（Device ID）
  - 设备制造商设定的序列号，不可修改，保证唯一
  - 例如：0001050001-NCS_IF105_89C7BA
- 设备位号（TAG）
  - 用户为标识操作而设定，可以修改
  - 例如：TT-001
- 设备地址
  - 在一个网段上唯一的地址，例如，32 或者 0x20，可以由组态软件设定
  - 地址有效范围，0x10~0xFB
  - 一般情况，0x10~0x13 为链路主设备预留，其他设备可以使用 0x14~0xF7 作为固定的地址，0xF8~0xFB 为临时地址
- 调度通信（Schedule Communication）



- 非调度通信（Unschedule Communication）



- 链路活动调度器（Link Active Scheduler）

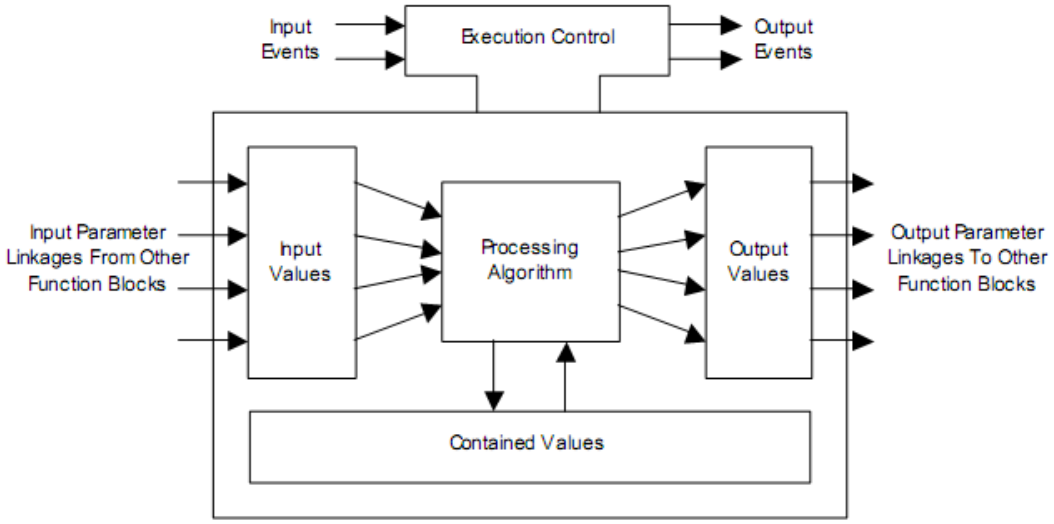


- 虚拟通信关系 VCR (Virtual Communication Relationship)
  - FAS 使用数据链路层的调度和非调度特性为 FMS 提供通信服务，这种类型的服务被称为虚拟通信关系 VCR(Virtual Communication Relationship)
  - FAS 支持三种类型的 VCR，即 client/server，publisher/subscriber 和 report distribution
- 三种 VCR 类型
  - client/server，数据在队列中，使用非调度通信，实现设备之间一对一的通信，主要用于设备功能块参数的读写访问
  - publisher/subscriber，数据在缓冲区，使用调度通信，主要用于设备功能块的输入输出参数之间交换数据，实现一对多通信
  - report distribution，数据在队列中，使用非调度通信，主要用于设备发送事件更新，报警数据，趋势数据等，实现一对多通信

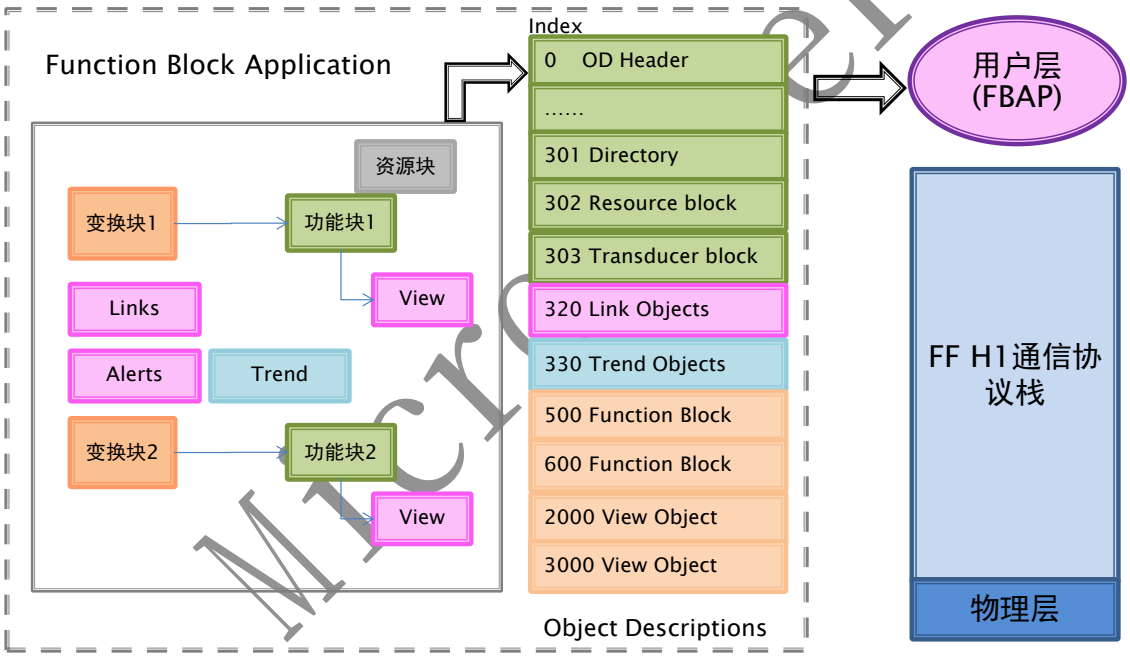
2. 功能块技术

- 资源块
  包含设备资源信息，如内存大小，厂商 ID 号等
- 变换块
  包含传感器相关信息，如量程，校准，线性化等。
- 功能块
  包括输入输出功能模块和算法控制模块，直接参与系统组态和控制。

- 功能块原理图



- 功能块应用结构图

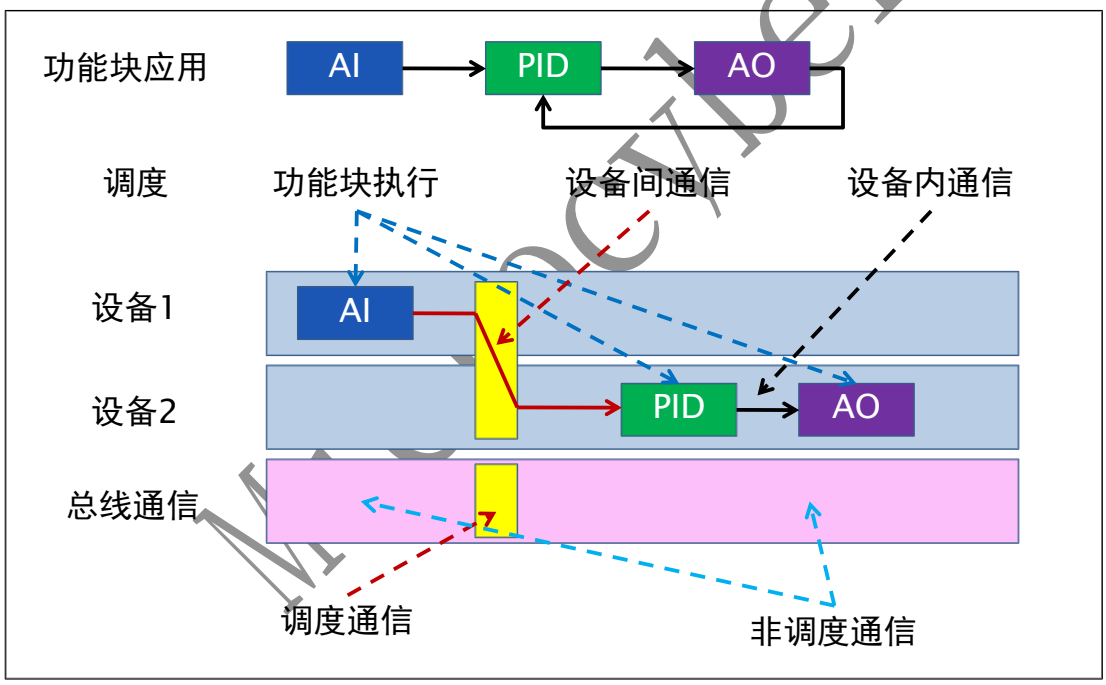


- 功能块种类

Part -2 Blocks	十个标准功能块	Part-3 Blocks	高级功能块
AI	Analog Input Block	DC	Device Control Block
DI	Discrete Input Block	OS	Output Splitter Block
ML	Manual Loader Block	SC	Signal Characterizer Block
BG	Bias/Gain Station Block	LL	Lead Lag Block
CS	Control Selector Block	DT	Dead Time Block

PD	P, PD Controller Block	IT	Integrator (Totalizer) Block
PID	PID, PI, I Controller Block	SPG	Setpoint Ramp Generator
RA	Ratio Station Block	IS	Input Selector
AO	Analog Output Block	AR	Arithmetic
DO	Discrete Output Block	TRM	Timer
Part-4 Blocks	**多路 I/O 功能块**	**Part-5 Blocks**	**IEC61131 Blocks**
MAI	Multiple Analog Input Block		Flexible Function Block
MDI	Multiple Discrete Input Block		
MAO	Multiple Analog Output Block		
MDO	Multiple Discrete Output Block		

- 功能块调度图



3. 设备的集成，EDD 和 CFF

- EDD 可以提供一个互操作环境，使 DCS 系统或者手操器可以获取现代自动化传感器和执行机构里面的信息用于：
  - 组态
  - 设备标定
  - 诊断问题
  - 提供显示在用户界面上的数据和报警
- 现在已经有了超过两千万的现场设备使用 EDD 技术连接各家厂商的主机。

- 标准化的 EDDL 作为一项标准语言用来描述：
  - 设备参数及依赖关系
  - 设备功能，例如仿真模式，标定
  - 图形化的表示，例如菜单，对话框
  - 与控制设备互动
- EDDL 用于创建 EDD，EDD 被控制系统以合适的工具用于实现参数组态，调整，操作及监视
- EDDL 被四大基金会认同
  - 现场总线基金会
  - HART 基金会
  - Profibus 基金会
  - OPC 基金会

- CFF（Common File Format 的缩写）是应用于离线组态工具的文本文件，包括
  - 设备标识信息
  - 通信协议栈网络管理和系统管理参数
  - 功能块目录索引信息
  - 功能块的类型和实例化信息
  - 功能块的参数默认值
  - .....

```
//================
// File Header
//================
[File Header]
FileType=CapabilitiesFile
FileDate= 2009,03,10
                // 10 March, 2009
Description="This is an example of a
Capabilities File of the FF TOOL KITS"
//==================
// Device Header
//==================
[Device Header]
[Device VFD 1]
// Each VFD contains the three
following attributes for FMS Identify.
VendorName="Microcyber Inc."
ModelName="FF-TOOL-KITS"
Revision="3.00.1.00"
```

附录三 FF 总线功能块参数简介

1. Resource Block

Index	Parameter Mnemonic	VIEW_ 1	VIEW_ 2	VIEW_ 3	VIEW_ 4
1	ST_REV	2	2	2	2
2	TAG_DESC				
3	STRATEGY				2
4	ALERT_KEY				1
5	MODE_BLK	4		4	
6	BLOCK_ERR	2		2	
7	RS_STATE	1		1	
8	TEST_RW				
9	DD_RESOURCE				
10	MANUFAC_ID				4
11	DEV_TYPE				2
12	DEV_REV				1
13	DD_REV				1
14	GRANT_DENY		2		
15	HARD_TYPES				2
16	RESTART				
17	FEATURES				2
18	FEATURE_SEL		2		
19	CYCLE_TYPE				2
20	CYCLE_SEL		2		
21	MIN_CYCLE_T				4
22	MEMORY_SIZE				2
23	NV_CYCLE_T		4		
24	FREE_SPACE		4		
25	FREE_TIME	4		4	
26	SHED_RCAS		4		
27	SHED_ROUT		4		
28	FAULT_STATE	1		1	
29	SET_FSTATE				
30	CLR_FSTATE				
31	MAX_NOTIFY				1
32	LIM_NOTIFY		1		
33	CONFIRM_TIME		4		

Index	Parameter Mnemonic	VIEW_ 1	VIEW_ 2	VIEW_ 3	VIEW_ 4
34	WRITE_LOCK		1		
35	UPDATE_EVT				
36	BLOCK_ALM				
37	ALARM_SUM	8		8	
38	ACK_OPTION				2
39	WRITE_PRI				1
40	WRITE_ALM				
41	ITK_VER				2
42	FD_VER				2
43	FD_FAIL_ACTIVE	4		4	
44	FD_OFFSPEC_ACTIVE	4		4	
45	FD_MAINT_ACTIVE	4		4	
46	FD_CHECK_ACTIVE	4		4	
47	FD_FAIL_MAP				4
48	FD_OFFSPEC_MAP				4
49	FD_MAINT_MAP				4
50	FD_CHECK_MAP				4
51	FD_FAIL_MASK				4
52	FD_OFFSPEC_MASK				4
53	FD_MAINT_MASK				4
54	FD_CHECK_MASK				4
55	FD_FAIL_ALM				
56	FD_OFFSPEC_ALM				
57	FD_MAINT_ALM				
58	FD_CHECK_ALM				
59	FD_FAIL_PRI				1
60	FD_OFFSPEC_PRI				1
61	FD_MAINT_PRI				1
62	FD_CHECK_PRI				1
63	FD_SIMULATE			9	
64	FD_RECOMMEN_ACT	2		2	
	Totals	40	30	49	69

2. Analog Input Block

Index	Parameter Mnemonic	VIEW_ 1	VIEW_ 2	VIEW_ 3	VIEW_ 4
1	ST_REV	2	2	2	2
2	TAG_DESC				
3	STRATEGY				2
4	ALERT_KEY				1
5	MODE_BLK	4		4	
6	BLOCK_ERR	2		2	
7	PV	5		5	
8	OUT	5		5	
9	SIMULATE				
10	XD_SCALE		11		
11	OUT_SCALE		11		
12	GRANT_DENY		2		
13	IO_OPTS				2
14	STATUS_OPTS				2
15	CHANNEL				2
16	L_TYPE				1
17	LOW_CUT				4
18	PV_FTIME				4
19	FIELD_VAL	5		5	
20	UPDATE_EVT				
21	BLOCK_ALM				
22	ALARM_SUM	8		8	
23	ACK_OPTION				2
24	ALARM_HYS				4
25	HI_HI_PRI				1
26	HI_HI_LIM				4
27	HI_PRI				1
28	HI_LIM				4
29	LO_PRI				1
30	LO_LIM				4
31	LO_LO_PRI				1
32	LO_LO_LIM				4
33	HI_HI_ALM				
34	HI_ALM				
35	LO_ALM				
36	LO_LO_ALM				
	Totals	31	26	31	46

3. Discrete Input Block

Index	Parameter Mnemonic	VIEW_ 1	VIEW_ 2	VIEW_ 3	VIEW_ 4
1	ST_REV	2	2	2	2
2	TAG_DESC				
3	STRATEGY				2
4	ALERT_KEY				1
5	MODE_BLK	4		4	
6	BLOCK_ERR	2		2	
7	PV_D	2		2	
8	OUT_D	2		2	
9	SIMULATE_D				
10	XD_STATE		2		
11	OUT_STATE		2		
12	GRANT_DENY		2		
13	IO_OPTS				2
14	STATUS_OPTS				2
15	CHANNEL				2
16	PV_FTIME				4
17	FIELD_VAL_D	2		2	
18	UPDATE_EVT				
19	BLOCK_ALM				
20	ALARM_SUM	8		8	
21	ACK_OPTION				
22	DISC_PRI				2
23	DISC_LIM				1
24	DISC_ALM				1
	Totals	22	8	22	19

4. AO Output Block

Index	Parameter Mnemonic	VIEW_ 1	VIEW_ 2	VIEW_ 3	VIEW_ 4
1	ST_REV	2	2	2	2
2	TAG_DESC				
3	STRATEGY				2
4	ALERT_KEY				1
5	MODE_BLK	4		4	
6	BLOCK_ERR	2		2	
7	PV	5		5	
8	SP	5		5	
9	OUT	5		5	
10	SIMULATE				
11	PV_SCALE		11		
12	XD_SCALE		11		
13	GRANT_DENY		2		
14	IO_OPTS				2
15	STATUS_OPTS				2
16	READBACK	5		5	
17	CAS_IN	5		5	
18	SP_RATE_DN				4
19	SP_RATE_UP				4
20	SP_HI_LIM		4		
21	SP_LO_LIM		4		
22	CHANNEL				2
23	FSTATE_TIME				4
24	FSTATE_VAL				4
25	BKCAL_OUT		5		
26	RCAS_IN		5		
27	SHED_OPT				1
28	RCAS_OUT		5		
29	UPDATE_EVT				
30	BLOCK_ALM				
	Totals	33	34	48	28

5. DO Output Block

Index	Parameter Mnemonic	VIEW_ 1	VIEW_ 2	VIEW_ 3	VIEW_ 4
1	ST_REV	2	2	2	2
2	TAG_DESC				
3	STRATEGY				2
4	ALERT_KEY				1
5	MODE_BLK	4		4	
6	BLOCK_ERR	2		2	
7	PV_D	2		2	
8	SP_D	2		2	
9	OUT_D	2		2	
10	SIMULATE_D				
11	PV_STATE		2		
12	XD_STATE		2		
13	GRANT_DENY		2		
14	O_OPTS				2
15	STATUS_OPTS				2
16	READBACK_D	2		2	
17	CAS_IN_D	2		2	
18	CHANNEL				2
19	FSTATE_TIME				4
20	FSTATE_VAL_D				1
21	BKCAL_OUT_D			2	
22	RCAS_IN_D			2	
23	SHED_OPT				1
24	RCAS_OUT_D			2	
25	UPDATE_EVT				
26	BLOCK_ALM				
	Totals	18	8	24	17

6. PID Control Block

Index	Parameter Mnemonic	VIEW_ 1	VIEW_ 2	VIEW_ 3	VIEW_ 4
1	ST_REV	2	2	2	2
2	TAG_DESC				
3	STRATEGY				2
4	ALERT_KEY				1
5	MODE_BLK	4		4	
6	BLOCK_ERR	2		2	
7	PV	5		5	
8	SP	5		5	
9	OUT	5		5	
10	PV_SCALE		11		
11	OUT_SCALE		11		
12	GRANT_DENY		2		
13	CONTROL_OPT				2
14	STATUS_OPTS				2
15	IN			5	
16	PV_FTIME				4
17	BYPASS		1		
18	CAS_IN	5		5	
19	SP_RATE_DN				4
20	SP_RATE_UP				4
21	SP_HI_LIM		4		
22	SP_LO_LIM		4		
23	GAIN				4
24	RESET				4
25	BAL_TIME				4
26	RATE				4
27	BKCAL_IN			5	
28	OUT_HI_LIM		4		
29	OUT_LO_LIM		4		
30	BKCAL_HYS				4
31	BKCAL_OUT			5	
32	RCAS_IN			5	
33	ROUT_IN			5	
34	SHED_OPT				1
35	RCAS_OUT			5	
36	ROUT_OUT			5	
37	TRK_SCALE				11

Index	Parameter Mnemonic	VIEW_ 1	VIEW_ 2	VIEW_ 3	VIEW_ 4
38	TRK_IN_D	2		2	
39	TRK_VAL	5		5	
40	FF_VAL			5	
41	FF_SCALE				11
42	FF_GAIN				4
43	UPDATE_EVT				
44	BLOCK_ALM				
45	ALARM_SUM	8		8	
46	ACK_OPTION				2
47	ALARM_HYS				4
48	HI_HI_PRI				1
49	HI_HI_LIM				4
50	HI_PRI				1
51	HI_LIM				4
52	LO_PRI				1
53	LO_LIM				4
54	LO_LO_PRI				1
55	LO_LO_LIM				4
56	DV_HI_PRI				1
57	DV_HI_LIM				4
58	DV_LO_PRI				1
59	DV_LO_LIM				4
60	HI_HI_ALM				
61	HI_ALM				
62	LO_ALM				
63	LO_LO_ALM				
64	DV_HI_ALM				
65	DV_LO_ALM				
	Totals	43	43	83	104

7. Bias/Gain Block

Index	Parameter Mnemonic	VIEW_ 1	VIEW_ 2	VIEW_ 3	VIEW_ 4
1	ST_REV	2	2	2	2
2	TAG_DESC				
3	STRATEGY				2
4	ALERT_KEY				1
5	MODE_BLK	4		4	
6	BLOCK_ERR	2		2	
7	SP	5		5	
8	OUT	5		5	
9	OUT_SCALE		11		
10	GRANT_DENY		2		
11	CONTROL_OPTS				2
12	STATUS_OPTS				2
13	IN_1			5	
14	CAS_IN	5		5	
15	SP_RATE_DN				4
16	SP_RATE_UP				4
17	SP_HI_LIM		4		
18	SP_LO_LIM		4		
19	GAIN				4
20	BAL_TIME				4
21	BKCAL_IN			5	
22	OUT_HI_LIM		4		
23	OUT_LO_LIM		4		
24	BKCAL_OUT			5	
25	RCAS_IN			5	
26	SHED_OPT				1
27	RCAS_OUT			5	
28	TRK_SCALE				11
29	TRK_IN_D	2		2	
30	TRK_VAL	5		5	
31	UPDATE_EVT				
32	BLOCK_ALM				
	Totals	30	31	55	37

8. Signal Characterizer Block

Index	Parameter Mnemonic	VIEW_ 1	VIEW_ 2	VIEW_ 3	VIEW_ 4
1	ST_REV	2	2	2	2
2	TAG_DESC				
3	STRATEGY				2
4	ALERT_KEY				1
5	MODE_BLK	4		4	
6	BLOCK_ERR	2		2	
7	OUT_1	5		5	
8	OUT_2	5		5	
9	X_RANGE		11		
10	Y_RANGE		11		
11	GRANT_DENY		2		
12	IN_1	5		5	
13	IN_2	5		5	
14	SWAP_2				1
15	CURVE_X				
16	CURVE_Y				
17	UPDATE_EVT				
18	BLOCK_ALM				
	Totals	28	26	28	6

9. Ratio Control Block

Index	Parameter Mnemonic	VIEW_ 1	VIEW_ 2	VIEW_ 3	VIEW_ 4
1	ST_REV	2	2	2	2
2	TAG_DESC				
3	STRATEGY				2
4	ALERT_KEY				1
5	MODE_BLK	4		4	
6	BLOCK_ERR	2		2	
7	PV	5		5	
8	SP	4		4	
9	OUT	5		5	
10	PV_SCALE		11		
11	OUT_SCALE		11		
12	GRANT_DENY		2		
13	CONTROL_OPTS				2
14	STATUS_OPTS				2
15	IN			5	
16	PV_FTIME				4
17	IN_1			5	
18	RA_FTIME				4
19	CAS_IN	5		5	
20	SP_RATE_DN				4
21	SP_RATE_UP				4
22	SP_HI_LIM		4		
23	SP_LO_LIM		4		
24	GAIN				4
25	BKCAL_IN			5	
26	OUT_HI_LIM		4		
27	OUT_LO_LIM		4		
28	BKCAL_OUT			5	
29	BAL_TIME				4
30	RCAS_IN			5	
31	SHED_OPT				1
32	RCAS_OUT			5	
33	TRK_SCALE				11
34	TRK_IN_D	2		2	
35	TRK_VAL	5		5	
36	UPDATE_EVT				
37	BLOCK_ALM				

Index	Parameter Mnemonic	VIEW_ 1	VIEW_ 2	VIEW_ 3	VIEW_ 4
38	ALARM_SUM	8		8	
39	ACK_OPTION				2
40	ALARM_HYS				4
41	HI_HI_PRI				1
42	HI_HI_LIM				4
43	HI_PRI				1
44	HI_LIM				4
45	LO_PRI				1
46	LO_LIM				4
47	LO_LO_PRI				1
48	LO_LO_LIM				4
49	DV_HI_PRI				1
50	DV_HI_LIM				4
51	DV_LO_PRI				1
52	DV_LO_LIM				4
53	HI_HI_ALM				
54	HI_ALM				
55	LO_ALM				
56	LO_LO_ALM				
57	DV_HI_ALM				
58	DV_LO_ALM				
	Totals	42	42	72	81

10.Lead Lag Block

Index	Parameter Mnemonic	VIEW_ 1	VIEW_ 2	VIEW_ 3	VIEW_ 4
1	ST_REV	2	2	2	2
2	TAG_DESC				
3	STRATEGY				2
4	ALERT_KEY				1
5	MODE_BLK	4		4	
6	BLOCK_ERR	2		2	
7	OUT	5		5	
8	OUT_RANGE		11		
9	GRANT_DENY		2		
10	STATUS_OPTS				2
11	IN	5		5	
12	FOLLOW	2		2	
13	LAG_TIME				4
14	LEAD_TIME				4
15	BAL_TIME				4
16	OUTAGE_LIM				4
17	UPDATE_EVT				
18	BLOCK_ALM				
	Totals	20	15	20	23

11.Integrator Block

Index	Parameter Mnemonic	VIEW_ 1	VIEW_ 2	VIEW_ 3	VIEW_ 4
1	ST_REV	2	2	2	2
2	TAG_DESC				
3	STRATEGY				2
4	ALERT_KEY				1
5	MODE_BLK	4		4	
6	BLOCK_ERR	2		2	
7	TOTAL_SP	4		4	
8	OUT	5		5	
9	OUT_RANGE		11		
10	GRANT_DENY		2		
11	STATUS_OPTS				2
12	IN_1	5		5	
13	IN_2	5		5	
14	OUT_TRIP	2		2	
15	OUT_PTRIP	2		2	
16	TIME_UNIT1		1		
17	TIME_UNIT2		1		
18	UNIT_CONV				4
19	PULSE_VAL1				4
20	PULSE_VAL2				4
21	REV_FLOW1	2		2	
22	REV_FLOW2	2		2	
23	RESET_IN	2		2	
24	STOTAL			4	
25	RTOTAL	4		4	
26	SRTOTAL			4	
27	SSP			4	
28	INTEG_TYPE				1
29	INTEG_OPTS				2
30	CLOCK_PER				4
31	PRE_TRIP				4
32	N_RESET	4		4	
33	PCT_INCL	4		4	
34	GOOD_LIM				4
35	UNCERT_LIM				4
36	OP_CMD_INT	1		1	

Index	Parameter Mnemonic	VIEW_ 1	VIEW_ 2	VIEW_ 3	VIEW_ 4
37	OUTAGE_LIM				4
38	RESET_CONFIRM	2		2	
39	UPDATE_EVT				
40	BLOCK_ALM				
	Totals	52	17	64	42

12.Input Selector Block

Index	Parameter Mnemonic	VIEW_ 1	VIEW_ 2	VIEW_ 3	VIEW_ 4
1	ST_REV	2	2	2	2
2	TAG_DESC				
3	STRATEGY				2
4	ALERT_KEY				1
5	MODE_BLK	4		4	
6	BLOCK_ERR	2		2	
7	OUT	5		5	
8	OUT_RANGE		11		
9	GRANT_DENY		2		
10	STATUS_OPTS				2
11	IN_1	5		5	
12	IN_2	5		5	
13	IN_3	5		5	
14	IN_4	5		5	
15	DISABLE_1	2		2	
16	DISABLE_2	2		2	
17	DISABLE_3	2		2	
18	DISABLE_4	2		2	
19	SELECT_TYPE				1
20	MIN_GOOD				1
21	SELECTED	2		2	
22	OP_SELECT	2		2	
23	UPDATE_EVT				
24	BLOCK_ALM				
	Totals	45	15	45	9

13.Arithmetic Block

Index	Parameter Mnemonic	VIEW_ 1	VIEW_ 2	VIEW_ 3	VIEW_ 4
1	ST_REV	2	2	2	2
2	TAG_DESC				
3	STRATEGY				2
4	ALERT_KEY				1
5	MODE_BLK	4		4	
6	BLOCK_ERR	2		2	
7	PV	5		5	
8	OUT	5		5	
9	PRE_OUT	5		5	
10	PV_SCALE		11		
11	OUT_RANGE		11		
12	GRANT_DENY		2		
13	INPUT_OPTS				2
14	IN			5	
15	IN_LO			5	
16	IN_1			5	
17	IN_2			5	
18	IN_3			5	
19	RANGE_HI				4
20	RANGE_LO				4
21	BIAS_IN_1				4
22	GAIN_IN_1				4
23	BIAS_IN_2				4
24	GAIN_IN_2				4
25	BIAS_IN_3				4
26	GAIN_IN_3				4
27	COMP_HI_LIM				4
28	COMP_LO_LIM				4
29	ARITH_TYPE				4
30	BAL_TIME				4
31	BIAS				4
32	GAIN				4
33	OUT_HI_LIM				4
34	OUT_LO_LIM				4
35	UPDATE_EVT				
36	BLOCK_ALM				
	Totals	23	26	28	68

14. Parameter Attribute Definitions

Parameter Mnemonic	Obj Type	Data Type/ Structure	Use/Model	Store	Size	Valid Range	Initial Value	Direction	Units	Permission	Mode	Other	Range Check
ACK_OPTION	S	Bit String	C/Contained	S	2	0: Auto Ack Disabled 1: Auto Ack Enabled	0		na	ALARM			
ALARM_HYS	S	Float	C/Contained	S	4	0 to 50 Percent	0.50%		%	ALARM		Positive	Yes
ALARM_SUM	R	DS-74	C/Alarm Summary	mix	8				na	ALARM			
ALERT_KEY	S	Unsigned8	C/Alert Key	S	1	1 to 255	0		none				Yes
BAL_TIME	S	Float	C/Contained	S	4	Positive	0		Sec	TUNE		Positive	
BIAS	S	Float	C/Contained	N	4	OUT_SCALE +/- 10%			OUT	See Note 1			Yes
BKCAL_HYS	S	Float	C/Contained	S	4	0 to 50 Percent	0.50%		%	TUNE		Positive	Yes
BKCAL_IN	R	DS-65	I/Back-Calculation Input	N	5			BKWD	OUT				
BKCAL_OUT	R	DS-65	O/Back-Calculation Output	D	5			BKWD	PV			Read only	
BKCAL_OUT_D	R	DS-66	O/Back-Calculation Output	D	2			BKWD	PV			Read only	
BKCAL_SEL_1	R	DS-65	O/Back-Calculation Output	D	5			BKWD	OUT			Read only	
BKCAL_SEL_2	R	DS-65	O/ Back-Calculation Output	D	5			BKWD	OUT			Read only	

Parameter Mnemonic	Obj Type	Data Type/ Structure	Use/Model	Store	Size	Valid Range	Initial Value	Direction	Units	Permission	Mode	Other	Range Check
BKCAL_SEL_3	R	DS-65	O/ Back-Calculation Output	D	5			BKWD	OUT			Read only	
BLOCK_ALM	R	DS-72	C/Alarm	D	13				na				
BLOCK_ERR	S	Bit String	C/Block Error	D	2				E			Read only	
BYPASS	S	Unsigned8	C/Contained	S	1	1: Off, 2: On	0		E		Man		
CAS_IN	R	DS-65	I/Cascade Input	N	5			FWD	PV				
CAS_IN_D	R	DS-66	I/Cascade Input	N	2			FWD	PV				
CHANNEL	S	Unsigned16	C/Channel	S	2	1 to Mfgr limit	0		none		O/S		Yes
CLR_FSTATE	S	Unsigned8	C/Contained	D	1	1: Off, 2: Clear	1		E	See Note 3			
CONFIRM_TIME	S	Unsigned32	C/Contained	S	4		640000		1/32 millisec	TUNE			Yes
CONTROL_OPTS	S	Bit String	C/Contained	S	2		0		na		O/S		
CYCLE_SEL	S	Bit String	C/Contained	S	2		0		na	See Note 4			
CYCLE_TYPE	S	Bit String	C/Contained	S	2	Set by mfgr			na			Read only	
DEV_REV	S	Unsigned8	C/Contained	S	1	Set by mfgr			none			Read only	
DEV_TYPE	S	Unsigned16	C/Contained	S	2	Set by mfgr			E			Read only	
DD_RESOURCE	S	Visible String	C/DD Resource	S	32		null		na			Read only	

Parameter Mnemonic	Obj Type	Data Type/ Structure	Use/Model	Store	Size	Valid Range	Initial Value	Direction	Units	Permission	Mode	Other	Range Check
DD_REV	S	Unsigned8	C/Contained	S	1	Set by mfgr			none			Read only	
DISC_ALM	R	DS-72	C/Alarm	D	13				PV				
DISC_LIM	S	Unsigned8	C/Contained	S	1	PV_STATE	0		PV	ALARM			Yes
DISC_PRI	S	Unsigned8	C/Alert Priority	S	1	0 to 15	0		none	ALARM			Yes
DV_HI_ALM	R	DS-71	C/Alarm	D	16				PV				
DV_HI_LIM	S	Float	C/Contained	S	4	0 to PV span, +INF	+INF		PV	ALARM			Yes
DV_HI_PRI	S	Unsigned8	C/Alert Priority	S	1	0 to 15	0		none	ALARM			Yes
DV_LO_ALM	R	DS-71	C/Alarm	D	16				PV				
DV_LO_LIM	S	Float	C/Contained	S	4	-INF, -PV span to 0	-INF		PV	ALARM			Yes
DV_LO_PRI	S	Unsigned8	C/Alert Priority	S	1	0 to 15	0		none	ALARM			Yes
FAULT_STATE	S	Unsigned8	C/Contained	N	1	1: Clear, 2: Active			E			Read only	
FEATURE_SEL	S	Bit String	C/Contained	S	2		Set by mfgr		na				
FEATURES	S	Bit String	C/Contained	S	2	Set by mfgr			na			Read only	
FF_GAIN	S	Float	C/Contained	S	4		0		none	TUNE	Man		
FF_SCALE	R	DS-68	C/Scaling	S	11		0-100%		FF		O/S		
FF_VAL	R	DS-65	I /Input	N	5			FWD	FF				
FIELD_VAL	R	DS-65	C/Contained	D	5				%			Read only	
FIELD_VAL_D	R	DS-66	C/Contained	D	2				On/Off			Read only	

Parameter Mnemonic	Obj Type	Data Type/ Structure	Use/Model	Store	Size	Valid Range	Initial Value	Direction	Units	Permission	Mode	Other	Range Check
FREE_SPACE	S	Float	C/Contained	D	4	0-100 Percent			%			Read only	
FREE_TIME	S	Float	C/Contained	D	4	0-100 Percent			%			Read only	
FSTATE_TIME	S	Float	C/Contained	S	4	Positive	0		Sec			Positive	
FSTATE_VAL	S	Float	C/Contained	S	4	PV_SCALE +/- 10%	0		PV				Yes
FSTATE_VAL_D	S	Unsigned8	C/Contained	S	1		0		PV				
GAIN	S	Float	C/Contained	S	4		0		none	TUNE			
GRANT_DENY	R	DS-70	C/Access Permission	S	2				na				
HARD_TYPES	S	Bit String	C/Contained	S	2	Set by mfgr			na			Read only	
HI_ALM	R	DS-71	C/Alarm	D	16				PV				
HI_HI_ALM	R	DS-71	C/Alarm	D	16				PV				
HI_HI_LIM	S	Float	C/Contained	S	4	PV_SCALE, +INF	+INF		PV	ALARM			Yes
HI_HI_PRI	S	Unsigned8	C/Alert Priority	S	1	0 to 15	0		none	ALARM			Yes
HI_LIM	S	Float	C/Contained	S	4	PV_SCALE, +INF	+INF		PV	ALARM			Yes
HI_PRI	S	Unsigned8	C/Alert Priority	S	1	0 to 15	0		none	ALARM			Yes
IO_OPTS	S	Bit String	C/Contained	S	2		0		na		O/S		
IN	R	DS-65	I/Primary Input	N	5			FWD	PV				
IN_1	R	DS-65	I/Input	N	5			FWD	See Note 7				
ITK_VER	S	Unsigned16	C/Contained	S	2	Set by FF			none			Read	

Parameter Mnemonic	Obj Type	Data Type/ Structure	Use/Model	Store	Size	Valid Range	Initial Value	Direction	Units	Permission	Mode	Other	Range Check
												only	
LIM_NOTIFY	S	Unsigned8	C/Contained	S	1	0 to MAX_NOTIFY	MAX_ NOTIFY		none	TUNE			Yes
L_TYPE	S	Unsigned8	C/Contained	S	1	1: Direct, 2: Indirect, 3: Ind Sqr Root	0		E		Man		
LOW_CUT	S	Float	C/Contained	S	4	Non-negative	0		OUT	TUNE		Positive	Yes
LO_ALM	R	DS-71	C/Alarm	D	16				PV				
LO_LIM	S	Float	C/Contained	S	4	-INF, PV_SCALE	-INF		PV	ALARM			Yes
LO_PRI	S	Unsigned8	C/Alert Priority	S	1	0 to 15	0		none	ALARM			Yes
LO_LO_ALM	R	DS-71	C/Alarm	D	16				PV				
LO_LO_LIM	S	Float	C/Contained	S	4	-INF, PV_SCALE	-INF		PV	ALARM			Yes
LO_LO_PRI	S	Unsigned8	C/Alert Priority	S	1	0 to 15	0		none	ALARM			Yes
MANUFAC_ID	S	Unsigned32	C/Contained	S	4	Enumeration; controlled by FF			none			Read only	
MAX_NOTIFY	S	Unsigned8	C/Contained	S	1	Set by mfgr			none			Read only	
MEMORY_SIZE	S	Unsigned16	C/Contained	S	2	Set by mfgr			Kbytes			Read only	
MIN_CYCLE_T	S	Unsigned32	C/Contained	S	4	Set by mfgr			1/32 millisec			Read only	
MODE_BLK	R	DS-69	C/Mode	mix	4	See MODE	O/S		na	See Note 1		Note 2	
NV_CYCLE_T	S	Unsigned32	C/Contained	S	4				1/32 millisec			Read only	

Parameter Mnemonic	Obj Type	Data Type/ Structure	Use/Model	Store	Size	Valid Range	Initial Value	Direction	Units	Permission	Mode	Other	Range Check
OUT	R	DS-65	O/Primary Output	N	5	OUT_SCALE +/- 10% See Note 6		FWD	OUT	See Note 1	Man		Yes
OUT_D	R	DS-66	O/Primary Output	N	2	OUT_STATE		FWD	OUT	See Note 1	Man		Yes
OUT_HI_LIM	S	Float	C/Contained	S	4	OUT_SCALE +/- 10%	100		OUT				Yes
OUT_LO_LIM	S	Float	C/Contained	S	4	OUT_SCALE +/- 10%	0		OUT				Yes
OUT_SCALE	R	DS-68	C/Scaling	S	11		0-100%		OUT		O/S		
OUT_STATE	S	Unsigned16	C/Contained	S	2		0		OUT				
PV	R	DS-65	C/Process Variable	D	5				PV			Read only	
PV_D	R	DS-66	C/Process Variable	D	2				PV			Read only	
PV_FTIME	S	Float	C/Contained	S	4	non-negative	0		Sec	TUNE		Positive	
PV_SCALE	R	DS-68	C/Scaling	S	11		0-100%		PV		O/S		
PV_STATE	S	Unsigned16	C/Contained	S	2		0		PV				
RA_FTIME	S	Float	C/Contained	S	4	Positive	0		Sec	TUNE		Positive	
RATE	S	Float	C/Contained	S	4	Positive	0		Sec	TUNE		Positive	
RCAS_IN	R	DS-65	C/Remote-Cascade In	N	5			FWD_R	PV				
RCAS_IN_D	R	DS-66	C/Remote-Cascade In	N	2			FWD_R	PV				
RCAS_OUT	R	DS-65	C/Remote-Cascade Out	D	5			BKWD_ R	PV			Read only	

Parameter Mnemonic	Obj Type	Data Type/ Structure	Use/Model	Store	Size	Valid Range	Initial Value	Direction	Units	Permission	Mode	Other	Range Check
RCAS_OUT_D	R	DS-66	C/Remote-Cascade Out	D	2			BKWD_ R	PV			Read only	
READBACK	R	DS-65	C/Contained	D	5				XD			Read only	
READBACK_D	R	DS-66	C/Contained	D	2				XD			Read only	
RESET	S	Float	C/Contained	S	4	Positive	+INF		Sec	TUNE		Positive	
RESTART	S	Unsigned8	C/Contained	D	1	See Note 5			E	See Note 4			
ROUT_IN	R	DS-65	C/Remote-Output In	N	5			FWD_R	OUT				
ROUT_OUT	R	DS-65	C/Remotr-Output Out	D	5			BKWD_ R	OUT			Read only	
RS_STATE	S	Unsigned8	C/Resource State	D	1	See Part 1 for enumeration			E			Read only	
SEL_1	R	DS-65	I/Cascade Input	N	5			FWD	OUT				
SEL_2	R	DS-65	I/Cascade Input	N	5			FWD	OUT				
SEL_3	R	DS-65	I/Cascade Input	N	5			FWD	OUT				
SEL_TYPE	S	Unsigned8	C/Contained	S	1	1: High, 2: Low, 3: Middle	0		E		Man		
SET_FSTATE	S	Unsigned8	C/Contained	D	1	1: Off, 2: Set	1		E	See Note 3			
SHED_OPT	S	Unsigned8	C/Shed Option	S	1	See SHED_OPT	0		E				
SHED_RCAS	S	Unsigned32	C/Contained	S	4		640000		1/32 millisec	TUNE			Yes

Parameter Mnemonic	Obj Type	Data Type/ Structure	Use/Model	Store	Size	Valid Range	Initial Value	Direction	Units	Permission	Mode	Other	Range Check
SHED_ROUT	S	Unsigned32	C/Contained	S	4		640000		1/32 millisec	TUNE			Yes
SIMULATE	R	DS-82	C/Simulate	D	11		disable		none				
SIMULATE_D	R	DS-83	C/Simulate	D	5		disable		none				
SP	R	DS-65	C/Setpoint	N	5	PV_SCALE +/- 10%			PV	See Note 1	Auto or Rout		Yes
SP_D	R	DS-66	C/Setpoint	N	2	PV_STATE			PV	See Note 1	Auto		
SP_HI_LIM	S	Float	C/Contained	S	4	PV_SCALE +/- 10%	100		PV				Yes
SP_LO_LIM	S	Float	C/Contained	S	4	PV_SCALE +/- 10%	0		PV				Yes
SP_RATE_DN	S	Float	C/Contained	S	4	Positive	+INF		PV/Sec			Positive	
SP_RATE_UP	S	Float	C/Contained	S	4	Positive	+INF		PV/Sec			Positive	
ST_REV	S	Unsigned16	C/Static Revision	S	2		0		none			Read only	
STATUS_OPTS	S	Bit String	C/Contained	S	2		0		na		O/S		
STRATEGY	S	Unsigned16	C/Strategy	S	2		0		none				
TAG_DESC	S	Octet String	C/Tag Description	S	32		spaces		na				
TEST_RW	R	DS-85	C/Test	D	112				none				
TRK_IN_D	R	DS-66	I/Input	N	2			FWD	On/Off				
TRK_SCALE	R	DS-68	C/Scaling	S	11		0-100%		TRK		O/S		
TRK_VAL	R	DS-65	I/Input	N	5				TRK				
UPDATE_EVT	R	DS-73	C/Event Update	D	1 4				na			Read only	

Parameter Mnemonic	Obj Type	Data Type/ Structure	Use/Model	Store	Size	Valid Range	Initial Value	Direction	Units	Permission	Mode	Other	Range Check
WRITE_ALM	R	DS-72	C/Alarm	D	1 3				none				
WRITE_LOCK	S	Unsigned8	C/Contained	S	1	1: Unlocked, 2: Locked	1		E	See Note 3			
WRITE_PRI	S	Unsigned8	C/Alert Priority	S	1	0 to 15	0		none	ALARM			Yes
XD_SCALE	R	DS-68	C/Scaling	S	11		0-100%		XD		O/S		
XD_STATE	S	Unsigned16	C/Contained	S	2		0		XD				

NOTE 1	Normally, the operator has permission to write these values, but PROGRAM or LOCAL remove that permission and grant it to a supervisory computer or a local control panel.
NOTE 2	MODE_BLK has a mixture of storage types. See the Mode parameter formal model in Part 1.
NOTE 3	The operator can control PROGRAM or LOCAL access to these values.
NOTE 4	Changing these parameters may be fatal to communication.
NOTE 5	1: Run, 2: Restart resource, 3: Restart with defaults, 4: Restart processor, 5-10: Restart with factory defaults.
NOTE 6	OUT will be restricted to OUT_SCALE+/- 10% where the OUT_SCALE parameter is defined in the block and the Control Option “No OUT limits in Manual” has not been selected.”
NOTE 7	Units are specific to the function block – see specific function block description..

15. Field Diagnostics Parameter Attribute Definitions

Parameter Mnemonic	Obj Type	Data Type/ Structure	Use/Model	Store	Size	Valid Range	Initial Value	Direction	Units	Permission	Mode	Other	Range Check
FD_CHECK_ACTIVE	S	Bit String	C/FD Active	D	4				na			Read only	
FD_CHECK_ALM	R	DS-87	C/Alarm	D	15				na				
FD_CHECK_MAP	S	Bit String	C/Contained	S	4				na	ALARM			
FD_CHECK_MASK	S	Bit String	C/Contained	S	4				na	ALARM			
FD_CHECK_PRI	S	Unsigned8	C/Alert Priority	S	1	0 - 15	0		na	ALARM			Yes
FD_EXTENDED_ACTIVE_n	S	Bit String	C/Contained	D	4				na			Read only	
FD_EXTENDED_MAP_n	S	Bit String	C/Contained	S	4				na				
FD_FAIL_ACTIVE	S	Bit String	C/FD Active	D	4				na			Read only	
FD_FAIL_ALM	R	DS-87	C/Alarm	D	15				na				
FD_FAIL_MAP	S	Bit String	C/Contained	S	4				na	ALARM			
FD_FAIL_MASK	S	Bit String	C/Contained	S	4				na	ALARM			
FD_FAIL_PRI	S	Unsigned8	C/Alert	S	1	0 - 15	0		na	ALARM			Yes

			Priority										
FD_MAINT_ACTIVE	S	Bit String	C/FD Active	D	4				na			Read only	
FD_MAINT_ALM	R	DS-87	C/Alarm	D	15				na				
FD_MAINT_MAP	S	Bit String	C/Contained	S	4				na	ALARM			
FD_MAINT_MASK	S	Bit String	C/Contained	S	4				na	ALARM			
FD_MAINT_PRI	S	Unsigned8	C/Alert Priority	S	1	0 - 15	0		na	ALARM			Yes
FD_OFFSPEC_ACTIVE	S	Bit String	C/FD Active	D	4				na			Read only	
FD_OFFSPEC_ALM	R	DS-87	C/Alarm	D	15				na				
FD_OFFSPEC_MAP	S	Bit String	C/Contained	S	4				na	ALARM			
FD_OFFSPEC_MASK	S	Bit String	C/Contained	S	4				na	ALARM			
FD_OFFSPEC_PRI	S	Unsigned8	C/Alert Priority	S	1	0 - 15	0		na	ALARM			Yes
FD_RECOMMEN_ACT	S	Unsigned16	C/Contained	D	2	1 – manf spec	0		na			Read only	
FD_SIMULATE	R	DS-89	C/FD Simulate	D	9		disabled		na				
FD_VER	S	Unsigned16	C/Contained	S	2				na			Read only	

16. Parameter Descriptions

ACK_OPTION Selection of whether alarms associated with the block will be automatically acknowledged.
ALARM_HYS Amount the PV must return within the alarm limits before the alarm condition clears. Alarm Hysteresis is expressed as a percent of the PV span .
ALARM_SUM The current alert status, unacknowledged states, unreported states, and disabled states of the alarms associated with the function block.
ALERT_KEY The identification number of the plant unit. This information may be used in the host for sorting alarms, etc.
BAL_TIME This specifies the time for the internal working value of bias or ratio to return to the operator set bias or ratio, in seconds. In the PID block, it may be used to specify the time constant at which the integral term will move to obtain balance when the output is limited and the mode is Auto, Cas, or RCas.
BIAS The bias value used in computing the function block output, expressed in engineering units.
BKCAL_HYS The amount that the output must change away from its output limit before the limit status is turned off, expressed as a percent of the span of the output.
BKCAL_IN The value and status from a lower block's BKCAL_OUT that is used to prevent reset windup and to initialize the control loop.
BKCAL_OUT The value and status required by an upper block's BKCAL_IN so that the upper block may prevent reset windup and provide bumpless transfer to closed loop control.

BKCAL_OUT_D The output value and status provided to an upstream discrete block. This information is used to provide bumpless transfer to closed loop control.
BKCAL_SEL_1 Control elector output value and status associated with SEL_1 input which is provided to BKCAL_IN of the block connected to SEL_1 in order to prevent reset windup.
BKCAL_SEL_2 Control selector output value and status associated with SEL_2 input which is provided to BKCAL_IN of the block connected to SEL_2 in order to prevent reset windup.
BKCAL_SEL_3 Control selector output value and status associated with SEL_3 input which is provided to BKCAL_IN of the block connected to SEL_3 in order to prevent reset windup.
BLOCK_ALM The block alarm is used for all configuration, hardware, connection failure or system problems in the block. The cause of the alert is entered in the subcode field. The first alert to become active will set the Active status in the Status attribute. As soon as the Unreported status is cleared by the alert reporting task, another block alert may be reported without clearing the Active status, if the subcode has changed.
BLOCK_ERR This parameter reflects the error status associated with the hardware or software components associated with a block. It is a bit string, so that multiple errors may be shown.
BYPASS The normal control algorithm may be bypassed through this parameter. When bypass is set, the setpoint value (in percent) will be directly transferred to the output. To prevent a bump on transfer to/from bypass, the setpoint will automatically be initialized to the output value or process variable, respectively, and the path broken flag will be set for one execution.
CAS_IN This parameter is the remote setpoint value, which must come from another Fieldbus block, or a DCS block through a defined link.
CAS_IN_D This parameter is the remote setpoint value of a discrete block, which must come from another Fieldbus block, or a DCS block through a defined link.
CHANNEL The number of the logical hardware channel that is connected to this I/O block. This information defines the transducer to be used going to or from the physical world.
CLR_FSTATE Writing a Clear to this parameter will clear the device fault state if the field condition, if any, has cleared.

CONFIRM_TIME The time the resource will wait for confirmation of receipt of a report before trying again. Retry shall not happen when CONFIRM_TIME = 0.
CONTROL_OPTS Options which the user may select to alter the calculations done in a control block.
CYCLE_SEL Used to select the block execution method for this resource.
CYCLE_TYPE Identifies the block execution methods available for this resource.
DD_RESOURCE String identifying the tag of the resource which contains the Device Description for this resource.
DD_REV Revision of the DD associated with the resource - used by an interface device to locate the DD file for the resource.
DEV_REV Manufacturer revision number associated with the resource - used by an interface device to locate the DD file for the resource.
DEV_TYPE Manufacturer's model number associated with the resource - used by interface devices to locate the DD file for the resource.
DISC_ALM The status and time stamp associated with the discrete alarm.
DISC_LIM State of discrete input which will generate an alarm.
DISC_PRI Priority of the discrete alarm.
DV_HI_ALM The status and time stamp associated with the high deviation alarm.
DV_HI_LIM

The setting of the high deviation alarm limit in engineering units.
DV_HI_PRI Priority of the high deviation alarm.
DV_LO_ALM The status and time stamp associated with the low deviation alarm.
DV_LO_LIM The setting of the low deviation alarm limit in engineering units.
DV_LO_PRI Priority of the low deviation alarm.
FAULT_STATE Condition set by loss of communication to an output block, fault promoted to an output block or a physical contact. When Fault State condition is set, Then output function blocks will perform their FSTATE actions.
FEATURE_SEL Used to select resource block options.
FEATURES Used to show supported resource block options.
FF_GAIN The gain that the feed forward inpt is multiplied by before it is added to the calculated control output.
FF_SCALE The feedforward input high and low scale values, engineering units code, and number of digits to the right of the decimal point.
FF_VAL The feed forward value and status.
FIELD_VAL Raw value of the field device in percent of thePV range, with a status reflecting the Transducer condition, before signal characterization (L_TYPE) or filtering (PV_FTIME).

FIELD_VAL_D Raw value of the field device discrete input, with a status reflecting the Transducer condition.
FREE_SPACE Percent of memory available for further configuration. Zero in a preconfigured resource.
FREE_TIME Percent of the block processing time that is free to process additional blocks.
FSTATE_TIME The time in seconds from detection of fault of the output block remote setpoint to the output action of the block output if the condition still exists.
FSTATE_VAL The preset analog SP value to use when fault occurs. This value will be used if the I/O option Fault State to value is selected.
FSTATE_VAL_D The preset discrete SP_D value to use when fault occurs. This value will be used if the I/O option Fault State to value is selected.
GAIN Dimensionless value used by the block algorithm in calculating the block output.
GRANT_DENY Options for controlling access of host computer and local control panels to operating, tuning and alarm parameters of the block.
HARD_TYPES The types of hardware available as channel numbers.
HI_ALM The status for high alarm and its associated time stamp.
HI_HI_ALM The status for high high alarm and its associated time stamp.
HI_HI_LIM The setting for high high alarm in engineering units.
HI_HI_PRI

Priority of the high high alarm.
HI_LIM The setting for high alarm in engineering units.
HI_PRI Priority of the high alarm.
IO_OPTS Options which the user may select to alter input and output block processing.
IN The primary input value of the block, required for blocks that filter the input to get the PV.
IN_1 Auxiliary input value to the block, used for other values than the PV.
ITK_VER Major revision number of the interoperability test case used in certifying this device as interoperable. The format and range of the version number is defined and controlled by the Fieldbus Foundation. Note: The value of this parameter will be zero (o) if the device has not been registered as interoperable by the FF.
LIM_NOTIFY Maximum number of unconfirmed alert notify messages allowed.
L_TYPE Determines if the values passed by the transducer block to the AI block may be used directly (Direct) or if the value is in different units and must be converted linearly (Indirect), or with square root (Ind Sqr Root), using the input range defined by the transducer and the associated output range.
LO_ALM The status of the low alarm and its associated time stamp.
LO_LIM The setting for the low alarm in engineering units.
LO_LO_ALM The status of the low low alarm and its associated time stamp.

LO_LO_LIM The setting of the low low alarm in engineering units.
LO_LO_PRI Priority of the low low alarm.
LO_PRI Priority of the low alarm.
LOW_CUT Limit used in square root processing. A value of zero percent of scale is used in block processing if the transducer value falls below this limit, in % of scale. This feature may be used to eliminate noise near zero for a flow sensor.
MANUFAC_ID Manufacturer identification number - used by an interface device to locate the DD file for the resource.
MAX_NOTIFY Maximum number of unconfirmed notify messages possible.
MEMORY_SIZE Available configuration memory in the empty resource. To be checked before attempting a download.
MIN_CYCLE_T Time duration of the shortest cycle interval of which the resource is capable.
MODE_BLK The actual, target, permitted, and normal modes of the block.
NV_CYCLE_T Minimum time interval specified by the manufacturer for writing copies of NV parameters to non-volatile memory. Zero means it will never be automatically copied. At the end of NV_CYCLE_TIME, only those parameters which have changed (as defined by the manufacturer) need to be updated in NVRAM
OUT The primary analog value calculated as a result of executing the function.
OUT_D

The primary discrete value calculated as a result of executing the function.
OUT_HI_LIM Limits the maximum output value.
OUT_LO_LIM Limits the minimum output value.
OUT_SCALE The high and low scale values, engineering units code, and number of digits to the right of the decimal point to be used in displaying the OUT parameter and parameters which have the same scaling as OUT.
OUT_STATE Index to the text describing the states of a discrete output.
PV Either the primary analog value for use in executing the function, or a process value associated with it. May also be calculated from the READBACK value of an AO block.
PV_D Either the primary discrete value for use in executing the function, or a process value associated with it. May also be calculated from the READBACK_D value of a DO block.
PV_FTIME Time constant of a single exponential filter for the PV, in seconds.
PV_SCALE The high and low scale values, engineering units code, and number of digits to the right of the decimal point to be used in displaying the PV parameter and parameters which have the same scaling as PV.
PV_STATE Index to the text describing the states of a discrete PV.
RA_FTIME Time constant of a single exponential filter for the value to be ratioed, in seconds.
RATE Defines the derivative time constant, in seconds.

RCAS_IN Target setpoint and status provided by a supervisory Host to a analog control or output block.
RCAS_IN_D Target setpoint and status provided by a supervisory Host to a discrete control or output block.
RCAS_OUT Block setpoint and status after ramping - provided to a supervisory Host for back calculation and to allow action to be taken under limiting conditions or mode change.
RCAS_OUT_D Block setpoint and status provided to a supervisory Host for back calculation and to allow action to be taken under limiting conditions or mode change.
READBACK This indicates the readback of the actual continuous valve or other actuator position, in transducer units.
READBACK_D This indicates the readback of the actual discrete valve or other actuator position, in the transducer state.
RESET The integral time constant, in seconds per repeat.
RESTART Allows a manual restart to be initiated. Several degrees of restart are possible. They are 1: Run, 2: Restart resource, 3: Restart with defaults, and 4: Restart processor.
ROUT_IN Target output and status provided by a Host to the control block for use as the output (ROut mode).
ROUT_OUT Block output and status - provided to a Host for back calculation in ROut mode and to allow action to be taken under limited conditions or mode change.
RS_STATE State of the function block application state machine.
SEL_1 First input value to the selector.
SEL_2

Second input value to the selector.
SEL_3 Third input value to the selector.
SEL_TYPE This parameter specifies the type of selector action, from choices of High, Medium, and Low.
SET_FSTATE Allows the Fault State condition to be manually initiated by selecting Set.
SHED_OPT Defines action to be taken on remote control device timeout.
SHED_RCAS Time duration at which to give up on computer writes to function block RCas locations. Shed from RCas shall never happen when SHED_RCAS = 0.
SHED_ROUT Time duration at which to give up on computer writes to function block ROut locations. Shed from Rout shall never happen when SHED_ROUT = 0.
SIMULATE Allows the transducer analog input or output to the block to be manually supplied when simulate is enabled. When simulation is disabled, the simulate value and status track the actual value and status.
SIMULATE_D Allows the transducer discrete input or output to the block to be manually supplied when simulate is enabled. When simulation is disabled, the simulate value and status track the actual value and status.
SP The analog setpoint of this block.
SP_D The discrete setpoint of this block.
SP_HI_LIM The setpoint high limit is the highest setpoint operator entry that can be used for the block.
SP_LO_LIM The setpoint low limit is the lowest setpoint operator entry that can be used for the block.

SP_RATE_DN Ramp rate at which downward setpoint changes are acted on in Auto mode, in PV units per second. If the ramp rate is set to zero, then the setpoint will be used immediately. For control blocks, rate limiting will apply only in Auto. For output blocks, rate limiting will apply in Auto, Cas, and RCas modes.
SP_RATE_UP Ramp rate at which upward setpoint changes are acted on in Auto mode, in PV units per second. If the ramp rate is set to zero, then the setpoint will be used immediately. For control blocks, rate limiting will apply only in Auto. For output blocks, rate limiting will apply in Auto, Cas, and RCas modes.
ST_REV The revision level of the static data associated with the function block. To support tracking changes in static parameter attributes, the associated block's static revision parameter will be incremented each time a static parameter attribute value is changed. Also, the associated block's static revision parameter may be incremented if a static parameter attribute is written but the value is not changed.
STATUS_OPTS Options which the user may select in the block processing of status.
STRATEGY The strategy field can be used to identify grouping of blocks.. This data is not checked or processed by the block.
TAG_DESC The user description of the intended application of the block.
TEST_RW Read/write test parameter - used only for conformance testing.
TRK_IN_D This discrete input is used to initiate external tracking of the block output to the value specified by TRK_VAL.
TRK_SCALE The high and low scale values, engineering units code, and number of digits to the right of the decimal point, associated with TRK_VAL.
TRK_VAL This input is used as the track value when external tracking is enabled by TRK_IN_D.
UPDATE_EVT This alert is generated by any change to the static data.

WRITE_ALM This alert is generated if the write lock parameter is cleared.
WRITE_LOCK If set, no writes from anywhere are allowed, except to clear WRITE_LOCK. Block inputs will continue to be updated.
WRITE_PRI Priority of the alarm generated by clearing the write lock.
XD_SCALE The high and low scale values, engineering units code, and number of digits to the right of the decimal point used with the value obtained from the transducer for a specified channel.
XD_STATE Index to the text describing the states of a discrete for the value obtained from the transducer.

17. Field Diagnostics Parameter Descriptions

FD_CHECK_PRI This parameter allows the user to specify the priority of this alarm category.
FD_EXTENDED_MAP_n An optional parameter or parameters to allow the user finer control on enabling conditions contributing to the conditions in FD_*_ACTIVE parameters.
FD_EXTENDED_ACTIVE_n An optional parameter or parameters to allow the user finer detail on conditions causing an active condition in the FD_*_ACTIVE parameters.
FD_FAIL_ACTIVE This parameter reflects the error conditions that are being detected as active as selected for this category. It is a bit string, so that multiple conditions may be shown.
FD_FAIL_ALM This parameter is used primarily to broadcast a change in the associated active conditions, which are not masked, for this alarm category to a Host System.

FD_FAIL_MAP This parameter maps conditions to be detected as active for this alarm category. Thus the same condition may be active in all, some, or none of the 4 alarm categories.
FD_FAIL_MASK This parameter allows the user to suppress any single or multiple conditions that ar e active, in this category, from being broadcast to the host through the alarm para meter. A bit equal to '1' will mask i.e. inhibit the broadcast of a condition, and a bit equal to '0' will unmask i.e. allow broadcast of a condition.
FD_FAIL_PRI This parameter allows the user to specify the priority of this alarm category.
FD_MAINT_ACTIVE This parameter reflects the error conditions that are being detected as active as selected for this category. It is a bit string, so that multiple conditions may be shown.
FD_MAINT_ALM This parameter is used primarily to broadcast a change in the associated active conditions, which are not masked, for this alarm category to a Host System.
FD_MAINT_MAP This parameter maps conditions to be detected as active for this alarm category. Thus the same condition may be active in all, some, or none of the 4 alarm categories.
FD_MAINT_MASK This parameter allows the user to suppress any single or multiple conditions that ar e active, in this category, from being broadcast to the host through the alarm para meter. A bit equal to '1' will mask i.e. inhibit the broadcast of a condition, and a bit equal to '0' will unmask i.e. allow broadcast of a condition.
FD_MAINT_PRI This parameter allows the user to specify the priority of this alarm category.